DRAM Package Electrical Specifications

Table 133: DRAM Package Electrical Specifications for x4 and x8 Devices

Parameter		Symbol	1600/1866/2133/2400/2666		2933		3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input/output	Zpkg	Z_{IO}	45	85	48	85	48	85	ohm	1, 2, 4
	Package delay	Td_{IO}	14	42	14	40	14	40	ps	1, 3, 4
	Lpkg	L_{IO}	–	3.3	–	3.3	–	3.3	nH	10
	Cpkg	C_{IO}	–	0.78	–	0.78	–	0.78	pF	11
DQS_t, DQS_c	Zpkg	$Z_{IO\ DQS}$	45	85	48	85	48	85	ohm	1, 2
	Package delay	$Td_{IO\ DQS}$	14	42	14	40	14	40	ps	1, 3
	Delta Zpkg	$DZ_{IO\ DQS}$	–	10	–	10	–	10	ohm	1, 2, 6
	Delta delay	$DTd_{IO\ DQS}$	–	5	–	5	–	5	ps	1, 3, 6
	Lpkg	$L_{IO\ DQS}$	–	3.3	–	3.3	–	3.3	nH	10
	Cpkg	$C_{IO\ DQS}$	–	0.78	–	0.78	–	0.78	pF	11
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	50	90	50	90	50	90	ohm	1, 2, 8
	Package delay	$Td_{I\ CTRL}$	14	42	14	40	14	40	ps	1, 3, 8
	Lpkg	$L_{I\ CTRL}$	–	3.4	–	3.4	–	3.4	nH	10
	Cpkg	$C_{I\ CTRL}$	–	0.7	–	0.7	–	0.7	pF	11
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	50	90	50	90	50	90	ohm	1, 2, 7
	Package delay	$Td_{I\ ADD\ CMD}$	14	45	14	40	14	40	ps	1, 3, 7
	Lpkg	$L_{I\ ADD\ CMD}$	–	3.6	–	3.6	–	3.6	nH	10
	Cpkg	$C_{I\ ADD\ CMD}$	–	0.74	–	0.74	–	0.74	pF	11
CK_t, CK_c	Zpkg	Z_{CK}	50	90	50	90	50	90	ohm	1, 2
	Package delay	Td_{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ_{DCK}	–	10	–	10	–	10	ohm	1, 2, 5
	Delta delay	DTd_{DCK}	–	5	–	5	–	5	ps	1, 3, 5
	Lpkg	$L_{I\ CLK}$	–	3.4	–	3.4	–	3.4	nH	10
	Cpkg	$C_{I\ CLK}$	–	0.7	–	0.7	–	0.7	pF	11
ZQ Zpkg		$Z_{O\ ZQ}$	–	100	–	100	–	100	ohm	1, 2
ZQ delay		$Td_{O\ ZQ}$	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		$Z_{O\ ALERT}$	40	100	40	100	40	100	ohm	1, 2
ALERT delay		$Td_{O\ ALERT}$	20	55	20	55	20	55	ps	1, 3

Notes: 1. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDQ},

V_{SS}, and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die, not pin, side.

2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).
3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
4. Z_{IO} and Td_{IO} apply to DQ, DM, TDQS_t and TDQS_c.
5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
6. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
7. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, WE_n, ACT_n, and PAR.
8. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
10. It is assumed that Lpkg can be approximated as Lpkg = Z_O × Td.
11. It is assumed that Cpkg can be approximated as Cpkg = Td/Z_O.

Table 134: DRAM Package Electrical Specifications for x16 Devices

Parameter		Symbol	1600/1866/2133/2400/2666		2933		3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input/output	Zpkg	Z_{IO}	45	85	45	85	45	85	ohm	1, 2, 4
	Package delay	Td_{IO}	14	45	14	45	14	45	ps	1, 3, 4
	Lpkg	L_{IO}	–	3.4	–	3.4	–	3.4	nH	11
	Cpkg	C_{IO}	–	0.82	–	0.82	–	0.82	pF	11
LDQS_t/LDQS_c/UDQS_t/UDQS_c	Zpkg	$Z_{IO\ DQS}$	45	85	45	85	45	85	ohm	1, 2
	Package delay	$Td_{IO\ DQS}$	14	45	14	45	14	45	ps	1, 3
	Lpkg	$L_{IO\ DQS}$	–	3.4	–	3.4	–	3.4	nH	11
	Cpkg	$C_{IO\ DQS}$	–	0.82	–	0.82	–	0.82	pF	11
LDQS_t/LDQS_c, UDQS_t/UDQS_c,	Delta Zpkg	$DZ_{IO\ DQS}$	–	10.5	–	10.5	–	10.5	ohm	1, 2, 6
	Delta delay	$DTd_{IO\ DQS}$	–	5	–	5	–	5	ps	1, 3, 6
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	50	90	50	90	50	90	ohm	1, 2, 8
	Package delay	$Td_{I\ CTRL}$	14	42	14	42	14	42	ps	1, 3, 8
	Lpkg	$L_{I\ CTRL}$	–	3.4	–	3.4	–	3.4	nH	11
	Cpkg	$C_{I\ CTRL}$	–	0.7	–	0.7	–	0.7	pF	11
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	50	90	50	90	50	90	ohm	1, 2, 7
	Package delay	$Td_{I\ ADD\ CMD}$	14	52	14	52	14	52	ps	1, 3, 7
	Lpkg	$L_{I\ ADD\ CMD}$	–	3.9	–	3.9	–	3.9	nH	11
	Cpkg	$C_{I\ ADD\ CMD}$	–	0.86	–	0.86	–	0.86	pF	11

Table 134: DRAM Package Electrical Specifications for x16 Devices (Continued)

Parameter		Symbol	1600/1866/2133/2400/2666		2933		3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
CK_t, CK_c	Zpkg	Z_{CK}	50	90	50	90	50	90	ohm	1, 2
	Package delay	Td_{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ_{DCK}	–	10.5	–	10.5	–	10.5	ohm	1, 2, 5
	Delta delay	DTd_{DCK}	–	5	–	5	–	5	ps	1, 3, 5
Input CLK	Lpkg	$L_{I\ CLK}$	–	3.4	–	3.4	–	3.4	nH	11
	Cpkg	$C_{I\ CLK}$	–	0.7	–	0.7	–	0.7	pF	11
ZQ Zpkg		$Z_{O\ ZQ}$	–	100	–	100	–	100	ohm	1, 2
ZQ delay		$Td_{O\ ZQ}$	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		$Z_{O\ ALERT}$	40	100	40	100	40	100	ohm	1, 2
ALERT delay		$Td_{O\ ALERT}$	20	55	20	55	20	55	ps	1, 3

Notes:
1. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die, not pin, side.
2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).
3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
4. Z_{IO} and Td_{IO} apply to DQ, DM, TDQS_t and TDQS_c.
5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
6. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
7. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, WE_n, ACT_n, and PAR.
8. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
10. It is assumed that Lpkg can be approximated as Lpkg = Z_O × Td.
11. It is assumed that Cpkg can be approximated as Cpkg = Td/Z_O.

Table 135: Pad Input/Output Capacitance

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400, 2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{IO}	0.55	1.4	0.55	1.15	0.55	1.00	0.55	1.00	pF	1, 2, 3
Input capacitance: CK_t and CK_c	C_{CK}	0.2	0.8	0.2	0.7	0.2	0.7	0.15	0.7	pF	2, 3
Input capacitance delta: CK_t and CK_c	C_{DCK}	-	0.05	-	0.05	-	0.05	-	0.05	pF	2, 3, 6
Input/output capacitance delta: DQS_t and DQS_c	C_{DDQS}	-	0.05	-	0.05	-	0.05	-	0.05	pF	2, 3, 5
Input capacitance: CTRL, ADD, CMD input-only pins	C_I	0.2	0.8	0.2	0.7	0.2	0.6	0.15	0.55	pF	2, 3, 4
Input capacitance delta: All CTRL input-only pins	C_{DI_CTRL}	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	2, 3, 8, 9
Input capacitance delta: All ADD/CMD input-only pins	$C_{DI\_ADD\_CMD}$	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 10, 11
Input/output capacitance delta: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{DIO}	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 3, 4
Input/output capacitance: ALERT pin	C_{ALERT}	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	2, 3
Input/output capacitance: ZQ pin	C_{ZQ}	–	2.3	–	2.3	–	2.3	–	2.3	pF	2, 3, 12
Input/output capacitance: TEN pin	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	0.15	2.3	pF	2, 3, 13

Notes:
1. Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The capacitance, if and when, is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). $V_{DD} = V_{DDQ} = 1.2V$, $V_{BIAS} = V_{DD}/2$ and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.
3. This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.
4. $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS\_t) + C_{IO}(DQS\_c))$.
5. Absolute value of C_{IO} (DQS_t), C_{IO} (DQS_c)
6. Absolute value of CCK_t, CCK_c
7. C_I applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
8. C_{DI_CTRL} applies to ODT, CS_n, and CKE.
9. $C_{DI\_CTRL} = C_I(CTRL) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$.
10. $C_{DI\_ADD\_CMD}$ applies to A[17:0], BA1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
11. $C_{DI\_ADD\_CMD} = C_I(ADD\_CMD) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$.
12. Maximum external load capacitance on ZQ pin: 5pF.
13. Only applicable if TEN pin does not have an internal pull-up.

Thermal Characteristics

Table 136: Thermal Characteristics

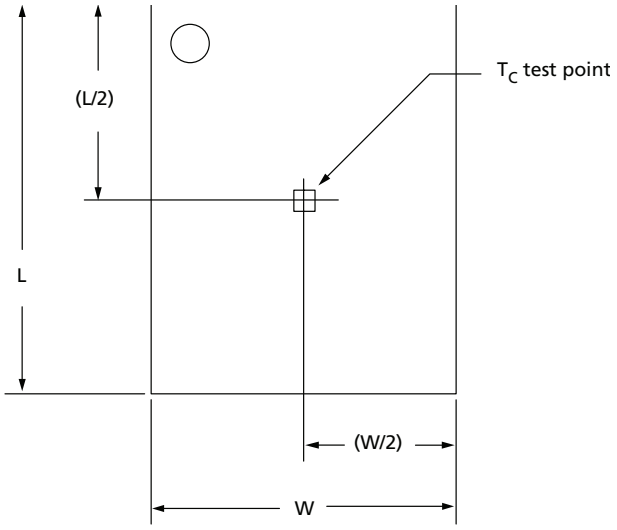
Parameter/Condition			Value	Units	Symbol	Notes
Operating case temperature: Commercial			0 to +85	°C	T_C	1, 2, 3
			0 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature: Industrial			–40 to +85	°C	T_C	1, 2, 3
			–40 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature: Automotive			–40 to +85	°C	T_C	1, 2, 3
			–40 to +105	°C	T_C	1, 2, 3, 4
REV A	78-ball "PM"	Junction-to-case (TOP)	3.1	°C/W	ΘJC	5
		Junction-to-board	10.6	°C/W	ΘJB	
	96-ball "HA"	Junction-to-case (TOP)	3.0	°C/W	ΘJC	5
		Junction-to-board	9.9	°C/W	ΘJB	
REV B	78-ball "WE"	Junction-to-case (TOP)	3.5	°C/W	ΘJC	5
		Junction-to-board	21	°C/W	ΘJB	
	96-ball "JY"	Junction-to-case (TOP)	4.1	°C/W	ΘJC	5
		Junction-to-board	16.2	°C/W	ΘJB	
REV D	78-ball "WE"	Junction-to-case (TOP)	3.2	°C/W	ΘJC	5
		Junction-to-board	20.2	°C/W	ΘJB	
	96-ball "LY"	Junction-to-case (TOP)	TBD	°C/W	ΘJC	5
		Junction-to-board	TBD	°C/W	ΘJB	
REV E	78-ball "SA"	Junction-to-case (TOP)	4.9	°C/W	ΘJC	5
		Junction-to-board	14.2	°C/W	ΘJB	
	96-ball "LY"	Junction-to-case (TOP)	4.8	°C/W	ΘJC	5
		Junction-to-board	15.2	°C/W	ΘJB	
REV G	78-ball "WE"	Junction-to-case (TOP)	2.8	°C/W	ΘJC	5
		Junction-to-board	13.1	°C/W	ΘJB	
	N/A	Junction-to-case (TOP)	N/A	°C/W	ΘJC	5
		Junction-to-board	N/A	°C/W	ΘJB	
REV H	78-ball "SA"	Junction-to-case (TOP)	4.4	°C/W	ΘJC	5
		Junction-to-board	13.2	°C/W	ΘJB	
	96-ball "LY"	Junction-to-case (TOP)	3.4	°C/W	ΘJC	5
		Junction-to-board	14.7	°C/W	ΘJB	
REV J	78-ball "SA"	Junction-to-case (TOP)	6.0	°C/W	ΘJC	5
		Junction-to-board	17.9	°C/W	ΘJB	
	96-ball "TB"	Junction-to-case (TOP)	5.9	°C/W	ΘJC	5
		Junction-to-board	17.4	°C/W	ΘJB	

Table 136: Thermal Characteristics (Continued)

Parameter/Condition			Value	Units	Symbol	Notes
REV R	78-ball "SA"	Junction-to-case (TOP)	8.2	°C/W	ΘJC	5
		Junction-to-board	19.8	°C/W	ΘJB	
	96-ball "TB"	Junction-to-case (TOP)	8.1	°C/W	ΘJC	5
		Junction-to-board	19.2	°C/W	ΘJB	

Notes: 1. MAX operating case temperature. T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate.
5. The thermal resistance data is based off of a typical number.

Figure 245: Thermal Measurement Point



Current Specifications – Measurement Conditions

I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

I_{DD}, I_{PP}, and I_{DDQ} measurement conditions, such as test load and patterns, are defined in this section.

- I_{DD} currents (I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5R}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7}, $_{DD8}$ and I_{DD9}) are measured as time-averaged currents with all V_{DD} balls of the device under test grouped together.
- I_{PP} currents are I_{PP3N} for standby cases (I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD8}), I_{PP0} for active cases (I_{DD0},I_{DD1}, I_{DD4R}, I_{DD4W}), I_{PP5R} for the distributed refresh case (I_{DD5R}), I_{PP6x} for self refresh cases (I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}), I_{PP7} for the operating bank interleave read case (I_{DD7}) and I_{PP9} for the MBIST-PPR operation case. These have the same definitions as the I_{DD} currents referenced but are measured on the V_{PP} supply.
- I_{DDQ} currents are measured as time-averaged currents with V_{DDQ} balls of the device under test grouped together. Micron does not specify I_{DDQ} currents.

- I_{PP} and I_{DDQ} currents are not included in I_{DD} currents, I_{DD} and I_{DDQ} currents are not included in I_{PP} currents, and I_{DD} and I_{PP} currents are not included in I_{DDQ} currents.

NOTE: I_{DDQ} values cannot be directly used to calculate the I/O power of the device. They can be used to support correlation of simulated I/O power to actual I/O power. In DRAM module application, I_{DDQ} cannot be measured separately because V_{DD} and V_{DDQ} are using a merged-power layer in the module PCB.

The following definitions apply for I_{DD}, I_{PP} and I_{DDQ} measurements.

- "0" and "LOW" are defined as $V_{IN} \leq V_{IL(AC)max}$
- "1" and "HIGH" are defined as $V_{IN} \geq V_{IH(AC)min}$
- "Midlevel" is defined as inputs $V_{REF} = V_{DD}/2$
- Timings used for I_{DD}, I_{PP} and I_{DDQ} measurement-loop patterns are provided in the Current Test Definition and Patterns section.
- Basic I_{DD}, I_{PP}, and I_{DDQ} measurement conditions are described in the Current Test Definition and Patterns section.
- Detailed I_{DD}, I_{PP}, and I_{DDQ} measurement-loop patterns are described in the Current Test Definition and Patterns section.
- Current measurements are done after properly initializing the device. This includes, but is not limited to, setting:
  $R_{ON} = R_{ZQ}/7$ (34 ohm in MR1);
  Qoff = 0B (output buffer enabled in MR1);
  $R_{TT(NOM)} = R_{ZQ}/6$ (40 ohm in MR1);
  $R_{TT(WR)} = R_{ZQ}/2$ (120 ohm in MR2);
  $R_{TT(Park)}$ = disabled;
  TDQS feature disabled in MR1; CRC disabled in MR2; CA parity feature disabled in MR3; Gear-down mode disabled in MR3; Read/Write DBI disabled in MR5; DM disabled in MR5
- Define D = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D_n = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

NOTE: The measurement-loop patterns must be executed at least once before actual current measurements can be taken, with the exception of IDD9 which may be measured any time after MBIST-PPR entry.

Figure 246: Measurement Setup and Test Load for I_{DDx}, I_{PPx}, and I_{DDQx}

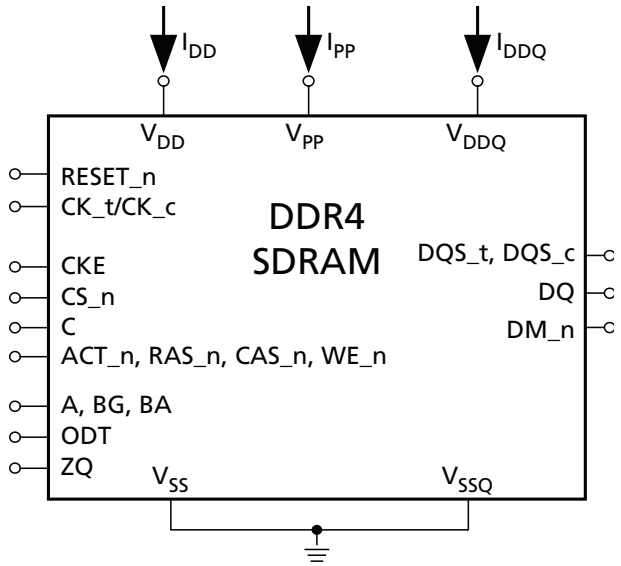
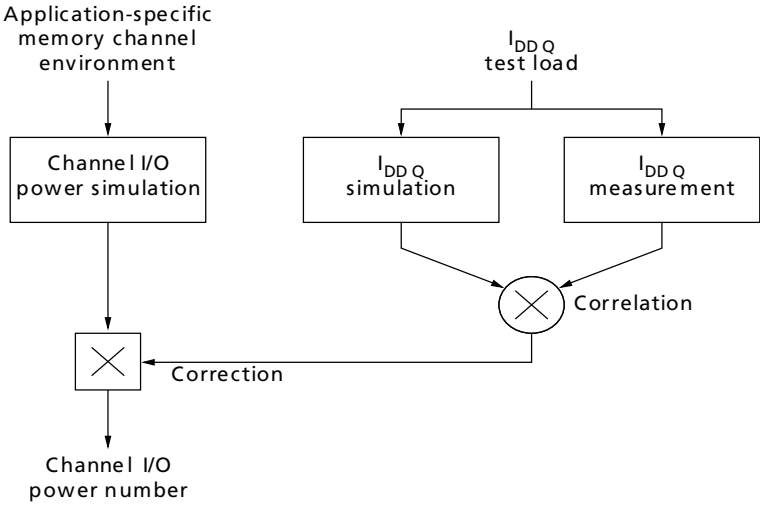


Figure 247: Correlation: Simulated Channel I/O Power to Actual Channel I/O Power



Note: 1. Supported by I_{DDQ} measurement.

I_{DD} Definitions

Table 137: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, *n*RC, *n*RAS, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: V_{DDQ}; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the I_{DD0} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD0} Measurement-Loop Pattern table

Table 137: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{PP0}	**Operating One Bank Active-Precharge I_{PP} Current (AL = 0)** Same conditions as I_{DD0} above
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, CL: see the previous table; BL: 8;[,, 5] AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the I_{DD1} Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Output buffer and R_{TT}: enabled in mode registers;[2] ODT Signal: stable at 0; Pattern details: see the I_{DD1} Measurement-Loop Pattern table
I_{DD2N}	**Precharge Standby Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{DD2NT}	**Precharge Standby ODT Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank gropup address, bank address inputs: partially toggling according to the I_{DD2NT} Measurement-Loop Pattern table; Data I/O: V_{SSQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: toggling according to the I_{DD2NT} Measurement-Loop Pattern table; Pattern details: see the I_{DD2NT} Measurement-Loop Pattern table
I_{DD2P}	**Precharge Power-Down Current** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{DD2Q}	**Precharge Quiet Standby Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{DD3N}	**Active Standby Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{PP3N}	**Active Standby I_{PP3N} Current (AL = 0)** Same conditions as I_{DD3N} above
I_{DD3P}	**Active Power-Down Current (AL = 0)** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0

Table 137: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD4R}	**Operating Burst Read Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[5] AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4R} Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the I_{DD4R} Measurement-Loop Pattern table; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the I_{DD4R} Measurement-Loop Pattern table); Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD4R} Measurement-Loop Pattern table
I_{DD4W}	**Operating Burst Write Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4W} Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the I_{DD4W} Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see I_{DD4W} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers (see note2); ODT signal: stable at HIGH; Pattern details: see the I_{DD4W} Measurement-Loop Pattern table
I_{DD5R}	**Distributed Refresh Current (1X REF)** CKE: HIGH; External clock: on; ^{t}CK, CL, *n*REFI: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD5R} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: REF command every *n*REFI (see the I_{DD5R} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers[2]; ODT signal: stable at 0; Pattern details: see the I_{DD5R} Measurement-Loop Pattern table
I_{PP5R}	**Distributed Refresh Current (1X REF)** Same conditions as I_{DD5R} above
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** T_C: 0–85°C; Auto self refresh (ASR): disabled;[3] Self refresh temperature range (SRT): normal;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{DD6E}	**Self Refresh Current: Extended Temperature Range [4]** T_C: 0–95°C; Auto self refresh (ASR): disabled[4]; Self refresh temperature range (SRT): extended;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, group bank address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{PP6x}	**Self Refresh I_{pp} Current** Same conditions as I_{DD6E} above
I_{DD6R}	**Self Refresh Current: Reduced Temperature Range** T_C: 0–45°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): reduced;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel

Table 137: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD7}	**Operating Bank Interleave Read Current** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, *n*RRD, *n*FAW, CL: see the previous table; BL: 8;[1, 5] AL: CL - 1; CS_n: HIGH between ACT and RDA; Command, address, group bank adress, bank address inputs: partially toggling according to the I_{DD7} Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the I_{DD7} Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the I_{DD7} Measurement-Loop Pattern table; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD7} Measurement-Loop Pattern table
I_{PP7}	**Operating Bank Interleave Read I_{PP} Current** Same conditions as I_{DD7} above
I_{DD8}	**Maximum Power Down Current** Place DRAM in MPSM then CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{DD9}	**MBIST-PPR Current [7]** Device in MBIST-PPR mode; External clock: on; CS_n: stable at 1 after MBIST-PPR entry; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{PP9}	**MBIST-PPR I_{PP} Current** Same condition with I_{DD9} above

Notes:
1. Burst length: BL8 fixed by MRS: set MR0[1:0] 00.
2. Output buffer enable: set MR1[12] 0 (output buffer enabled); set MR1[2:1] 00 (R_{ON} = R_{ZQ}/7); $R_{TT(NOM)}$ enable: set MR1[10:8] 011 (R_{ZQ}/6); $R_{TT(WR)}$ enable: set MR2[11:9] 001 (R_{ZQ}/2), and $R_{TT(Park)}$ enable: set MR5[8:6] 000 (disabled).
3. Auto self refresh (ASR): set MR2[6] 0 to disable or MR2[6] 1 to enable feature.
4. Self refresh temperature range (SRT): set MR2[7] 0 for normal or MR2[7] 1 for extended temperature range.
5. READ burst type: Nibble sequential, set MR0[3] 0.
6. In the dual-rank DDP case, note the following I_{DD} measurement considerations:
   - For all I_{DD} measurements except I_{DD6}, the unselected rank should be in an I_{DD2P} condition.
   - For all I_{PP} measurements except I_{PP6}, the unselected rank should be in an I_{DD3N} condition.
   - For all I_{DD6}/I_{PP6} measurements, both ranks should be in the same I_{DD6} condition.
7. When measuring I_{DD9}/I_{PP9} after entering MBIST-PPR mode and ALERT_N driving LOW, there is a chance that the DRAM may perform an internal hPPR if fails are found after internal self-test is completed and before ALERT_N fires HIGH.

Current Specifications – Patterns and Test Conditions

Current Test Definitions and Patterns

Table 138: I_{DD0} and I_{PP0} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			*n*RAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	–
			...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary															
		1	1 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	2 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	5 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	6 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	7 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	8 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	9 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	10 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	11 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	12 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	13 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	14 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	15 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ}.
4. For x4 and x8 only.

Table 139: I_{DD1} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 1...4 until *n*RCD - AL - 1; truncate if necessary															
			*n*RCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			*n*RAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary															
		1	1 × *n*RC + 0	ACT	0	0	0	1	1	0	1	1	0	0	0	0	0	0	–
			1 × *n*RC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1 × *n*RC + 3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern *n*RC + 1...4 until 1 × *n*RC + *n*RAS - 1; truncate if necessary															
			1 × *n*RC+*n*RCD - AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			1 × *n*RC + *n*RAS	PRE	0	1	0	1	0	0	1	1	0	0	0	0	0	0	
			...	Repeat pattern *n*RC + 1...4 until 2 × *n*RC - 1; truncate if necessary															
		2	2 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	5 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	6 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	7 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	9 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	10 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	11 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	12 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	13 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															

Table 139: I_{DD1} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	13	14 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	15 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	16 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.
4. For x4 and x8 only.

Table 140: I_{DD2N}, I_{DD3N}, and I_{PP3P} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.

2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ}.
4. For x4 and x8 only.

Table 141: I_{DD2NT} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{SSQ}.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{SSQ}.
4. For x4 and x8 only.

Table 142: I_{DD4R} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			2, 3	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
		1	4	RD	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6, 7	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. BG1 is a "Don't Care" for x16 devices.
3. Burst sequence driven on each DQ signal by a READ command. Outside burst operation, DQ signals are V_{DDQ}.
4. For x4 and x8 only.

Table 143: I_{DD4W} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			2, 3	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		1	4	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			6, 7	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. BG1 is a "Don't Care" for x16 devices.
3. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.
4. For x4 and x8 only.

Table 144: I_{DD4Wc} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D8 = CRC
			1, 2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			3, 4	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		1	5	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00 D8 = CRC
			6, 7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			8, 9	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		2	10–14	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	15–19	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	20–24	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	25–29	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	30–34	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	35–39	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	40–44	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	45–49	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	50–54	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	55–59	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	60–64	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	65–69	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	70–74	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	75–79	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. Pattern provided for reference only.
2. DQS_t, DQS_c are V_{DDQ} when not toggling.
3. BG1 is a "Don't Care" for x16 devices.
4. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.
5. For x4 and x8 only.

Table 145: I_{DD5R} Measurement – Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	–
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			4	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			5–8	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 1 instead															
			9–12	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 2 instead															
			13–16	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 3 instead															
			17–20	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 1 instead															
			21–24	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 2 instead															
			25–28	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 3 instead															
			29–32	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 0 instead															
			33–36	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
			37–40	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
			41–44	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
			45–48	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
			49–52	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
			53–56	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
			57–60	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
			61–64	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															
		2	65...*n*REFI - 1	Repeat sub-loop 1; truncate if necessary															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ}.
4. For x4 and x8 only.

Table 146: I_{DD7} Measurement – Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	RDA	0	1	1	0	1	0	0	0	0	0	1	0	0	0	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 2...3 until *n*RRD - 1, if *n*RRD > 4. Truncate if necessary															
		1	*n*RRD	ACT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	–
			*n*RRD+1	RDA	0	1	1	0	1	0	1	1	0	0	1	0	0	0	
			...	Repeat pattern 2...3 until 2 × *n*RRD - 1, if *n*RRD > 4. Truncate if necessary															
		2	2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RRD	Repeat pattern 2...3 until *n*FAW - 1, if *n*FAW > 4 × *n*RRD. Truncate if necessary															
		5	*n*FAW	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		9	*n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		10	2 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead															
		11	2 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead															
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead															
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead															
		14	2 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		15	3 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead															
		16	3 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead															
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead															
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead															
		19	3 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		20	4 × *n*FAW	Repeat pattern 2...3 until *n*RC - 1, if *n*RC > 4 × *n*FAW. Truncate if necessary															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.
4. For x4 and x8 only.

I_{DD} Specifications

Table 147: Timings used for I_{DD}, I_{PP}, and I_{DDQ} Measurement – Loop Patterns

Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400			DDR4-2666			DDR4-2933			DDR4-3200			Unit
		10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	16-16-16	17-17-17	18-18-18	18-18-18	19-19-19	20-20-20	20-20-20	21-21-21	22-22-22	20-20-20	22-22-22	24-24-24	
^{t}CK		1.25			1.071			0.937			0.833			0.75			0.682			0.625			ns
CL		10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	20	21	22	20	22	24	CK
CWL		9	11	11	10	12	12	11	14	14	16	16	16	18	18	18	14	18	18	16	20	20	CK
*n*RCD		10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	19	20	21	20	22	24	CK
*n*RC		38	39	40	44	45	46	50	51	52	55	56	57	61	62	63	66	67	68	72	74	76	CK
*n*RP		10	11	12	12	13	14	14	15	16	16	17	18	18	19	20	19	20	21	20	22	24	CK
*n*RAS		28			32			36			39			43			47			52			CK
*n*FAW	x4[1]	16			16			16			16			16			16			16			CK
	x8	20			22			23			26			28			31			34			CK
	x16	28			28			32			36			40			44			48			CK
*n*RRD_S	x4	4			4			4			4			4			4			4			CK
	x8	4			4			4			4			4			4			4			CK
	x16	5			6			6			7			8			8			9			CK
*n*RRD_L	x4	5			5			6			6			7			8			8			CK
	x8	5			5			6			6			7			8			8			CK
	x16	6			6			7			8			9			10			11			CK
*n*CCD_S		4			4			4			4			4			4			4			CK
*n*CCD_L		5			5			6			6			7			8			8			CK
*n*WTR_S		2			3			3			3			4			4			4			CK
*n*WTR_L		6			7			8			9			10			11			12			CK
*n*REFI		6,240			7,283			8,325			9,364			10,400			11,437			12,480			CK
*n*RFC 2Gb		128			150			171			193			214			235			256			CK
*n*RFC 4Gb		208			243			278			313			347			382			416			CK
*n*RFC 8Gb		280			327			374			421			467			514			560			CK
*n*RFC 16Gb		280			327			374			421			467			514			560			CK

Notes: 1. 1KB based x4 use same numbers of clocks for *n*FAW as the x8.

Current Specifications – Limits

Table 148: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. A (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
I_{DD0}: One bank ACTIVATE-to-PRE-CHARGE current	x4, x8	55	60	65	TBD	mA
	x16	85	90	95	TBD	mA
I_{PP0}: One bank ACTIVATE-to-PRE-CHARGE I_{PP} current	x4, x8	3	3	3	TBD	mA
	x16	4	4	4	TBD	mA
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	x4, x8	70	75	80	TBD	mA
	x16	105	110	115	TBD	mA
I_{DD2N}: Precharge standby current	x4, x8	45	50	55	TBD	mA
	x16	65	70	75	TBD	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	55	60	65	TBD	mA
	x16	75	80	90	TBD	mA
I_{DD2P}: Precharge power-down current	x4, x8	25	30	35	TBD	mA
	x16	45	50	55	TBD	mA
I_{DD2Q}: Precharge quiet standby current	x4, x8	45	45	50	TBD	mA
	x16	65	65	70	TBD	mA
I_{DD3N}: Active standby current	x4, x8	55	55	60	TBD	mA
	x16	75	75	85	TBD	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	TBD	mA
I_{DD3P}: Active power-down current	x4, x8	35	40	40	TBD	mA
	x16	55	60	65	TBD	mA
I_{DD4R}: Burst read current	x4	135	145	160	TBD	mA
	x8	150	150	175	TBD	mA
	x16	210	230	250	TBD	mA
I_{DD4W}: Burst write current	x4	135	145	160	TBD	mA
	x8	150	160	175	TBD	mA
	x16	210	230	250	TBD	mA
I_{DD5R}: Distributed refresh current (1X REF)	x4, x8	64	64	68	TBD	mA
	x16	84	84	94	TBD	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	TBD	mA
I_{DD6N}: Self refresh current; 0–85°C [1]	ALL	30	30	30	TBD	mA
I_{DD6E}: Self refresh current; 0–95°C [2, 4]	x4, x8	35	35	35	TBD	mA
	x16	50	50	50		mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	ALL	25	25	25	TBD	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	20	20	20	TBD	mA

Table 148: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. A (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	25	25	25	TBD	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	x4, x8	35	35	35	TBD	mA
	x16	50	50	50	TBD	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C[25]	ALL	5	5	5		mA
I_{DD7}: Bank interleave read current	x4	250	255	265	TBD	mA
	x8	200	205	215	TBD	mA
	x16	265	270	280	TBD	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	25	25	25	TBD	mA
	x8	15	15	15	TBD	
	x16	20	20	20	TBD	mA
I_{DD8}: Maximum power-down current	ALL	20	20	20	TBD	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
22. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
24. The I_{DD} values must be derated (increased) when operated outside of the range 0°C ≤ T_C ≤ 85°C:
    When T_C < 0°C: I_{DD2P}, and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by 11%.

When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.

25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 149: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. B (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	52	55	58	61	64	mA
	x8	57	60	63	66	69	mA
	x16	95	100	105	110	115	mA
I_{DD2N}: Precharge standby current	ALL	33	34	35	36	37	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	45	50	50	55	60	mA
	x16	67	75	75	78	81	mA
I_{DD2P}: Precharge power-down current	ALL	25	25	25	25	25	mA
I_{DD2Q}: Precharge quiet standby current	ALL	30	30	30	30	30	mA
I_{DD3N}: Active standby current	x4	35	38	41	44	47	mA
	x8	40	43	46	49	52	mA
	x16	44	47	50	53	56	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	30	32	34	36	38	mA
	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA
I_{DD4R}: Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I_{DD4W}: Burst write current	x4	95	103	112	121	130	mA
	x8	115	123	132	141	150	mA
	x16	213	228	244	261	278	mA
I_{DD5R}: Distributed refresh current (1X REF)	x4, x8	50	53	56	59	62	mA
	x16	56	59	61	64	67	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA

Table 149: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. B (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6N}: Self refresh current; 0–85°C [1]	ALL	30	30	30	30	30	mA
I_{DD6E}: Self refresh current; 0–95°C [2, 4]	ALL	35	35	35	35	35	mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	ALL	20	20	20	20	20	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	20	20	20	20	20	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	30	30	30	30	30	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C[25]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	175	185	200	215	230	mA
	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	16	17	18	19	20	mA
	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I_{DD8}: Maximum power-down current	ALL	25	25	25	25	25	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).

18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
22. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
24. The I_{DD} values must be derated (increased) when operated outside of the range $0°C \le T_C \le 85°C$:
    When $T_C < 0°C$: I_{DD2P}, and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by 11%.
    When $T_C > 85°C$: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.
25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 150: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. D ($0° \le T_C \le 85°C$)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	52	55	58	61	64	mA
	x8	57	60	63	66	69	mA
	x16	95	100	105	110	115	mA
I_{DD2N}: Precharge standby current	ALL	33	34	35	36	37	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	45	50	50	55	60	mA
	x16	67	75	75	78	81	mA
I_{DD2P}: Precharge power-down current	ALL	25	25	25	25	25	mA
I_{DD2Q}: Precharge quiet standby current	ALL	30	30	30	30	30	mA
I_{DD3N}: Active standby current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	56	mA
	x16	49	52	55	58	61	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	30	32	34	36	38	mA
	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA

Table 150: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. D (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD4R}: Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I_{DD4W}: Burst write current	x4	105	113	122	130	140	mA
	x8	125	132	142	150	160	mA
	x16	225	240	255	270	290	mA
I_{DD5R}: Distributed refresh current (1X REF)	x4, x8	56	58	61	64	66	mA
	x16	61	64	67	69	72	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; 0–85°C [1]	ALL	31	31	31	31	31	mA
I_{DD6E}: Self refresh current; 0–95°C [2, 4]	ALL	36	36	36	36	36	mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	31	31	31	31	31	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C[25]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	175	185	200	215	230	mA
	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	16	17	18	19	20	mA
	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I_{DD8}: Maximum power-down current	ALL	25	25	25	25	25	mA

Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.

6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
22. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
24. The I_{DD} values must be derated (increased) when operated outside of the range $0°C \le T_C \le 85°C$:
    When $T_C < 0°C$: I_{DD2P}, and I_{DD3P} must be derated by +6%; I_{DD4R} and I_{DD4W} must be derated by +4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by +11%.
    When $T_C > 85°C$: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, and I_{DD4W} must be derated by +3%; I_{DD2P} must be derated by +40%; and I_{DD5R} and I_{PP5R} must be derated by +40%. These values are verified by design and characterization, and may not be subject to production test.
25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 151: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E ($-40° \le T_C \le 85°C$)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	37	39	41	43	45	mA
	x8	39	41	43	45	47	mA
	x16	46	48	50	52	54	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	50	52	54	56	58	mA
	x8	55	57	59	61	63	mA
	x16	72	74	76	78	80	mA
I_{DD2N}: Precharge standby current	ALL	29	30	31	32	33	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	36	38	40	42	44	mA
	x16	43	46	49	52	55	mA
I_{DD2P}: Precharge power-down current	ALL	22	22	22	22	22	mA
I_{DD2Q}: Precharge quiet standby current	ALL	26	26	26	26	26	mA

Table 151: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD3N}: Active standby current	x4	34	36	38	40	42	mA
	x8	35	37	39	41	43	mA
	x16	36	38	40	42	44	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	28	29	30	31	32	mA
	x8	29	30	31	32	33	mA
	x16	30	31	32	33	34	mA
I_{DD4R}: Burst read current	x4	110	120	131	142	153	mA
	x8	135	145	156	167	178	mA
	x16	235	253	273	293	312	mA
I_{DD4W}: Burst write current	x4	96	105	114	123	132	mA
	x8	114	123	132	141	150	mA
	x16	182	199	216	233	250	mA
I_{DD5R}: Distributed refresh current (1X REF)	ALL	46	47	48	49	50	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; -40–85°C [1]	ALL	34	34	34	34	34	mA
I_{DD6E}: Self refresh current; -40–95°C [2, 4]	ALL	58	58	58	58	58	mA
I_{DD6R}: Self refresh current; -40–45°C [3, 4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	31	31	31	31	31	mA
I_{DD6A}: Auto self refresh current (95°C)[4]	ALL	58	58	58	58	58	mA
I_{PP6x}: Auto self refresh I_{PP} current; -40–95°C[26]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	175	185	200	215	230	mA
	x8	170	175	180	185	190	mA
	x16	234	243	252	261	270	mA

Table 151: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{PP7}: Bank interleave read I_{PP} current	x4	14	14	14	14	14	mA
	x8	13	13	13	13	13	mA
	x16	18	18	18	18	18	mA
I_{DD8}: Maximum power-down current	ALL	18	18	18	18	18	mA

Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +8%(x4/x8), +7%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –6%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –30%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12%.
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
21. When 2X REF is enabled for I_{PP5R}, current changes by approximately +0%.
22. When 4X REF is enabled for I_{PP5R}, current changes by approximately +0%.
23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
24. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
26. The I_{DD} values must be derated (increased) when operating between 85°C < T_C ≤ 95°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, and I_{DD4W} must be derated by +3%; I_{DD2P} must be derated by +10%; and I_{DD5R} and I_{PP5R} must be derated by +43%; All I_{PP} currents except I_{PP6x} and I_{PP5R} must be derated by +0%. These values are verified by design and characterization, and may not be subject to production test.
27. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 152: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 105°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x8	43	45	47	49	51	mA
	x16	50	52	54	56	58	mA

Table 152: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 105°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x8	59	61	63	65	67	mA
	x16	77	79	81	83	85	mA
I_{DD2N}: Precharge standby current	ALL	32	33	34	35	36	mA
I_{DD2NT}: Precharge standby ODT current	x8	40	42	44	46	48	mA
	x16	47	49	53	56	59	mA
I_{DD2P}: Precharge power-down current	ALL	26	26	26	26	26	mA
I_{DD2Q}: Precharge quiet standby current	ALL	29	29	29	29	29	mA
I_{DD3N}: Active standby current	x8	39	41	43	45	47	mA
	x16	40	42	44	46	48	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x8	33	34	35	36	37	mA
	x16	34	35	36	37	38	mA
I_{DD4R}: Burst read current	x8	145	155	166	178	189	mA
	x16	247	265	292	306	326	mA
I_{DD4W}: Burst write current	x8	123	132	141	151	160	mA
	x16	193	210	228	245	263	mA
I_{DD5R}: Distributed refresh current (1X REF)	ALL	96	97	98	99	100	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; -40–85°C [1]	ALL	34	34	34	34	34	mA
I_{DD6E}: Self refresh current; -40–105°C [2, 4]	ALL	95	95	95	95	95	mA
I_{DD6R}: Self refresh current; -40–45°C [3, 4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	31	31	31	31	31	mA

Table 152: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. E (-40° ≤ T_C ≤ 105°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6A}: Auto self refresh current (105°C)[4]	ALL	95	95	95	95	95	mA
I_{PP6x}: Auto self refresh I_{PP} current; -40–105°C[26]	ALL	6	6	6	6	6	mA
I_{DD7}: Bank interleave read current	x8	175	180	185	190	195	mA
	x16	239	248	257	266	275	mA
I_{PP7}: Bank interleave read I_{PP} current	x8	13	13	13	13	13	mA
	x16	18	18	18	18	18	mA
I_{DD8}: Maximum power-down current	ALL	20	20	20	20	20	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–105°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +8%(x4/x8), +7%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –6%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –30%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12%.
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
21. When 2X REF is enabled for I_{PP5R}, current changes by approximately +0%.
22. When 4X REF is enabled for I_{PP5R}, current changes by approximately +0%.
23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
24. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.

26. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 153: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	57	mA
	x16	75	80	85	90	95	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	52	55	58	61	64	mA
	x8	57	60	63	66	69	mA
	x16	95	100	105	110	115	mA
I_{DD2N}: Precharge standby current	ALL	33	34	35	36	37	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	45	50	50	55	60	mA
	x16	67	75	75	78	81	mA
I_{DD2P}: Precharge power-down current	ALL	25	25	25	25	25	mA
I_{DD2Q}: Precharge quiet standby current	ALL	30	30	30	30	30	mA
I_{DD3N}: Active standby current	x4	40	43	46	49	52	mA
	x8	45	48	51	54	56	mA
	x16	49	52	55	58	61	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	30	32	34	36	38	mA
	x8	35	37	39	41	43	mA
	x16	39	41	43	45	47	mA
I_{DD4R}: Burst read current	x4	100	110	121	132	143	mA
	x8	125	135	146	157	168	mA
	x16	225	243	263	283	302	mA
I_{DD4W}: Burst write current	x4	100	108	117	126	135	mA
	x8	120	128	137	146	155	mA
	x16	218	233	249	266	283	mA
I_{DD5R}: Distributed refresh current (1X REF)	x4, x8	56	58	61	64	66	mA
	x16	61	64	67	69	72	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; 0–85°C [1]	ALL	31	31	31	31	31	mA

Table 153: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6E}: Self refresh current; 0–95°C [2, 4]	ALL	36	36	36	36	36	mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.6	8.6	8.6	8.6	8.6	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	21	21	21	21	21	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	31	31	31	31	31	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C[25]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	175	185	200	215	230	mA
	x8	170	175	180	185	190	mA
	x16	239	249	259	269	279	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	16	17	18	19	20	mA
	x8	15	15	15	15	15	mA
	x16	20	20	20	20	20	mA
I_{DD8}: Maximum power-down current	ALL	25	25	25	25	25	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –23%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.

21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
22. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
24. The I_{DD} values must be derated (increased) when operated outside of the range $0°C \le T_C \le 85°C$:
    When $T_C < 0°C$: I_{DD2P}, and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by 11%.
    When $T_C > 85°C$: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.
25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 154: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. H ($0° \le T_C \le 85°C$)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	55	55	57	60	na	mA
	x8	55	55	60	61	na	mA
	x16	75	75	80	83	na	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	na	mA
	x16	5	5	5	5	na	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	68	68	71	75	na	mA
	x8	68	68	73	75	na	mA
	x16	100	100	107	111	na	mA
I_{DD2N}: Precharge standby current	ALL	39	39	42	43	na	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	43	43	48	50	na	mA
	x16	47	47	50	54	na	mA
I_{DD2P}: Precharge power-down current	ALL	27	27	27	27	na	mA
I_{DD2Q}: Precharge quiet standby current	ALL	34	34	36	36	na	mA
I_{DD3N}: Active standby current	x4	46	47	49	52	na	mA
	x8	46	47	49	52	na	mA
	x16	46	47	50	53	na	mA
I_{PP3N}: Active standby I_{PP} current	ALL	4.5	4.5	4.5	4.5	na	mA
I_{DD3P}: Active power-down current	x4	34	34	34	37	na	mA
	x8	36	36	39	40	na	mA
	x16	37	37	40	42	na	mA
I_{DD4R}: Burst read current	x4	135	135	157	173	na	mA
	x8	147	147	174	188	na	mA
	x16	259	259	312	341	na	mA

Table 154: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. H (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD4W}: Burst write current	x4	163	163	192	210	na	mA
	x8	181	181	217	234	na	mA
	x16	298	298	359	392	na	mA
I_{DD5R}: Distributed refresh current (1X REF)	x4	49	49	51	53	na	mA
	x8	49	49	51	53	na	mA
	x16	49	49	52	54	na	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5.5	5.5	5.5	5.5	na	mA
I_{DD6N}: Self refresh current; 0–85°C [1]	ALL	36	36	36	36	na	mA
I_{DD6E}: Self refresh current; 0–95°C [2, 4]	x4, x8	48	48	49	49	na	mA
	x16	50	50	50	51	na	mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	ALL	26	26	26	26	na	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	15	15	15	15	na	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	26	26	26	26	na	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	36	36	36	36	na	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C[25]	ALL	5	5	5	5	na	mA
I_{DD7}: Bank interleave read current	x4	278	278	388	369	na	mA
	x8	228	228	240	244	na	mA
	x16	311	311	321	331	na	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	21	21	26	28	na	mA
	x8	16	16	16	16	na	mA
	x16	22	22	22	22	na	mA
I_{DD8}: Maximum power-down current	ALL	21	21	21	21	na	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%(x4/x8), +4%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately 0%.

8. When DLL is disabled for I_{DD2N}, current changes by approximately –5%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –25%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +7%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +3%(x4/x8), +4%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately +10%(x4/x8), +10%(x16).
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12% (x8), +12% (x16).
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately –14%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately –33%.
21. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
22. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
23. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
24. The I_{DD} values must be derated (increased) when operated outside of the range $0°C \le T_C \le 85°C$:
    When $T_C < 0°C$: I_{DD2P}, and I_{DD3P} must be derated by 6%; I_{DD4R} and I_{DD4W} must be derated by 4%; I_{DD6}, I_{DD6ET}, and I_{DD7} must be derated by 11%.
    When $T_C > 85°C$: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5R} must be derated by 3%; I_{DD2P} must be derated by 40%. These values are verified by design and characterization, and may not be subject to production test.
25. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 155: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. J (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	35	37	39	41	43	mA
	x8	37	39	41	43	44	mA
	x16	44	46	48	50	52	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	3	3	3	3	3	mA
	x16	4	4	4	4	4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	48	50	51	53	55	mA
	x8	52	54	56	58	60	mA
	x16	68	70	72	74	76	mA
I_{DD2N}: Precharge standby current	ALL	28	29	30	30	31	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	34	36	38	40	42	mA
	x16	41	44	47	50	53	mA
I_{DD2P}: Precharge power-down current	ALL	22	22	22	22	22	mA
I_{DD2Q}: Precharge quiet standby current	ALL	26	26	26	26	26	mA

Table 155: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. J (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD3N}: Active standby current	x4	34	36	38	40	42	mA
	x8	35	37	39	41	43	mA
	x16	36	38	40	42	44	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	28	29	30	31	32	mA
	x8	29	30	31	32	33	mA
	x16	30	31	32	33	34	mA
I_{DD4R}: Burst read current	x4	105	114	125	135	145	mA
	x8	128	138	148	158	169	mA
	x16	223	240	260	278	296	mA
I_{DD4W}: Burst write current	x4	91	100	108	117	126	mA
	x8	108	116	125	134	142	mA
	x16	173	189	205	221	238	mA
I_{DD5R}: Distributed refresh current (1X REF)	ALL	44	45	45	46	47	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; -40–85°C [1]	ALL	32	32	32	32	32	mA
I_{DD6E}: Self refresh current; -40–95°C [2, 4]	ALL	55	55	55	55	55	mA
I_{DD6R}: Self refresh current; -40–45°C [3, 4]	ALL	20	20	20	20	20	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8.2	8.2	8.2	8.2	8.2	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	20	20	20	20	20	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	30	30	30	30	30	mA
I_{DD6A}: Auto self refresh current (95°C)[4]	ALL	55	55	55	55	55	mA
I_{PP6x}: Auto self refresh I_{PP} current; -40–95°C[27]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	166	176	190	205	219	mA
	x8	161	166	171	175	180	mA
	x16	222	231	240	248	257	mA

Table 155: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. J (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{PP7}: Bank interleave read I_{PP} current	x4	11	11	11	11	11	mA
	x8	10	10	10	10	13	mA
	x16	15	15	15	15	15	mA
I_{DD8}: Maximum power-down current	ALL	18	18	18	18	18	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +8%(x4/x8), +7%(x16).
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +1%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately –6%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –20%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +13%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +2%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4(x4/x8), +3%(x16).
14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%(x4/x8), -20%(x16).
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +4%(x4/x8), +3%(x16).
16. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +12%.
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
21. When 2X REF is enabled for I_{PP5R}, current changes by approximately +0%.
22. When 4X REF is enabled for I_{PP5R}, current changes by approximately +0%.
23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
24. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
26. The I_{DD} values must be derated (increased) when operating between 85°C < T_C ≤ 95°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, and I_{DD4W}, must be derated by +3%; I_{DD2P} must be derated by +13%; I_{DD5R} and I_{PP5R} must be derated by +43%; All I_{PP} currents except I_{PP6x} and I_{PP5R} must be derated by +0%. These values are verified by design and characterization, and may not be subject to production test.
27. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Table 156: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. R (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	38	40	42	44	46	mA
	x8	40	42	44	46	48	mA
	x16	51	53	55	57	59	mA

Table 156: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. R (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	x4, x8	4	4	4	4	4	mA
	x16	5	5	5	5	5	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	43	45	47	49	51	mA
	x8	47	49	51	53	55	mA
	x16	61	63	65	67	69	mA
I_{DD2N}: Precharge standby current	ALL	34	35	36	37	38	mA
I_{DD2NT}: Precharge standby ODT current	x4, x8	33	35	37	39	41	mA
	x16	38	40	42	44	46	mA
I_{DD2P}: Precharge power-down current	ALL	30	30	30	30	30	mA
I_{DD2Q}: Precharge quiet standby current	ALL	34	34	34	34	34	mA
I_{DD3N}: Active standby current	x4	34	36	38	40	42	mA
	x8	35	37	39	41	43	mA
	x16	36	38	40	42	44	mA
I_{PP3N}: Active standby I_{PP} current	ALL	3	3	3	3	3	mA
I_{DD3P}: Active power-down current	x4	28	29	30	31	32	mA
	x8	29	30	31	32	33	mA
	x16	30	31	32	33	34	mA
I_{DD4R}: Burst read current	x4	74	80	88	95	103	mA
	x8	92	98	105	113	123	mA
	x16	130	139	151	164	176	mA
I_{DD4W}: Burst write current	x4	62	66	70	76	82	mA
	x8	79	85	91	98	106	mA
	x16	102	109	119	127	138	mA
I_{DD5R}: Distributed refresh current (1X REF)	ALL	44	45	45	46	47	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	ALL	5	5	5	5	5	mA
I_{DD6N}: Self refresh current; -40–85°C [1]	ALL	32	32	32	32	32	mA
I_{DD6E}: Self refresh current; -40–95°C [2, 4]	ALL	52	52	52	52	52	mA
I_{DD6R}: Self refresh current; -40–45°C [3, 4]	ALL	19	19	19	19	19	mA

Table 156: I_{DD}, I_{PP}, and I_{DDQ} Current Limits; Die Rev. R (-40° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	8	8	8	8	8	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	19	19	19	19	19	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	29	29	29	29	29	mA
I_{DD6A}: Auto self refresh current (95°C)[4]	ALL	52	52	52	52	52	mA
I_{PP6x}: Auto self refresh I_{PP} current; -40–95°C[27]	ALL	5	5	5	5	5	mA
I_{DD7}: Bank interleave read current	x4	154	169	186	200	215	mA
	x8	135	140	145	150	155	mA
	x16	165	179	196	210	225	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	13	13	13	13	13	mA
	x8	8	8	8	8	8	mA
	x16	13	13	13	13	13	mA
I_{DD8}: Maximum power-down current	ALL	24	24	24	24	24	mA
I_{DD9}: MBIST-PPR current	ALL	170	170	170	170	170	mA
I_{PP9}: MBIST-PPR I_{PP} current	ALL	13	13	13	13	13	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (-40–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (-40–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (-40–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately 2%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately +19%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately -20%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately +2%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately -2%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +6%.
16. When write DBI is enabled for I_{DD4W}, current changes by approximately +1%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +14%.
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately 0%.

20. When 4X REF is enabled for I_{DD5R}, current changes by approximately 0%.
21. When 2X REF is enabled for I_{PP5R}, current changes by approximately 0%.
22. When 4X REF is enabled for I_{PP5R}, current changes by approximately 0%.
23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
24. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
26. The I_{DD} values must be derated (increased) when operating between 85°C < T_C ≤ 95°C: I_{DD0}, I_{DD1}, I_{DD2N} ,I_{DD2P} ,I_{DD2NT} ,I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, and I_{DD4W}, must be derated by +10%. I_{DD5R} and I_{PP5R} must be derated by +43%; I_{PP0} must be derated by +13%. I_{PP3N} must be derated by +22%. I_{PP7} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.
27. I_{PP6x} is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Speed Bin Tables

DDR4 DRAM timing is primarily covered by two types of tables: the Speed Bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The timing parameter tables define the applicable timing specifications based on the speed rating. The Speed Bin tables on the following pages list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given speed mark and are applicable to the CL settings in the lower half of the table provided they are applied in the correct clock range, which is noted.

Backward Compatibility

Although the speed bin tables list the slower data rates, ^{t}AA, CL, and CWL, it is difficult to determine whether a faster speed bin supports all of the ^{t}AA, CL, and CWL combinations across all the data rates of a slower speed bin. To assist in this process, please refer to the Backward Compatibility table.

Table 157: Backward Compatibility

Note 1 applies to the entire table.

Component Speed Bin	Speed Bin Supported																	
	-125	-125E	-107	-107E	-093	-093E	-083D	-083	-083E	-075D	-075	-075E	-068D	-068	-068E	-062	-062E	-062Y
-125	yes																	
-125E	yes[2]	yes																
-107	yes		yes															
-107E	yes[2]	yes	yes[2]	yes														
-093	yes		yes		yes													
-093E	yes[2]	yes	yes[2]	yes	yes[2]	yes												
-083D	yes		yes		yes		yes											
-083	yes		yes		yes		yes	yes										
-083E	yes[2]	yes	yes[2]	yes	yes[2]	yes	yes[2]	yes[2]	yes									
-075D	yes		yes		yes		yes			yes								
-075	yes		yes		yes		yes	yes		yes	yes							
-075E	yes	yes	yes	yes	yes	yes	yes	yes		yes	yes	yes						
-068D	yes		yes		yes		yes			yes			yes					
-068	yes		yes		yes		yes	yes		yes	yes		yes	yes				
-068E	yes		yes		yes		yes	yes		yes	yes		yes	yes	yes			
-062	yes		yes		yes		yes			yes			yes			yes		
-062E	yes		yes		yes		yes	yes		yes	yes		yes	yes		yes	yes	
-062Y	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes		yes	yes	yes

Notes: 1. The backward compatibility table is not meant to guarantee that any new device will be a drop in replacement for an existing part number. Customers should review the operating conditions for any device to determine its suitability for use in their design.
2. This condition exceeds the JEDEC requirement in order to allow additional flexibility for components. However, JEDEC SPD compliance may force modules to only support the JEDEC-defined value. Refer to the SPD documentation for further clarification.

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Table 158: DDR4-1600 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-1600 Speed Bin							-125E		-125		
CL-*n*RCD-*n*RP							11-11-11		12-12-12		
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ command to first data						^{t}AA	13.75 (13.50)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						$^{t}AA\_DBI$	^{t}AA (MIN) + 2*n*CK	^{t}AA (MAX) + 2*n*CK	^{t}AA (MIN) + 2*n*CK	^{t}AA (MAX) + 2*n*CK	ns
ACTIVATE-to-internal READ or WRITE delay time						^{t}RCD	13.75 (13.50)[4]	–	15.00	–	ns
PRECHARGE command period						^{t}RP	13.75 (13.50)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	35	9 × $^{t}REFI$	35	9 × $^{t}REFI$	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin(ns): non-DB**	**READ CL: nonDBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	-	13.50	9	11	9	^{t}CK (AVG)	1.500	1.900[6]	Reserved		ns
	-	15.00	10	12		^{t}CK (AVG)	1.500[6]	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)			1.250	<1.500	ns
Supported CL settings							9, 10[6], 11-12		10, 12		*n*CK
Supported CL settings with read DBI							11, 12[6], 13-14		12, 14		*n*CK
Supported CWL settings							9, 11		9, 11		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 159: DDR4-1866 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-1866 Speed Bin							-107E		-107		
CL-*n*RCD-*n*RP							13-13-13		14-14-14		
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ command to first data						^{t}AA	13.92 (13.50)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						^{t}AA_DBI	^{t}AA (MIN) + 2*n*CK	^{t}AA (MAX) + 2*n*CK	^{t}AA (MIN) + 2*n*CK	^{t}AA (MAX) + 2*n*CK	ns
ACTIVATE to internal READ or WRITE delay time						^{t}RCD	13.92 (13.50)[4]	–	15.00	–	ns
PRECHARGE command period						^{t}RP	13.92 (13.50)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	34	9 × ^{t}REFI	34	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin: nonDBI**	**READ CL: nonDBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	–	13.50	9	11	9	^{t}CK (AVG)	1.500	1.900[6]	Reserved		ns
	–	15.00	10	12		^{t}CK (AVG)	1.500[6]	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)			1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^{t}CK (AVG)	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^{t}CK (AVG)			1.071	<1.250	ns
Supported CL settings							9, 10[6], 11–14		10, 12, 14		*n*CK
Supported CL settings with read DBI							11, 12[6], 13–16		12, 14, 16		*n*CK
Supported CWL settings							9–12		9–12		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

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3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 160: DDR4-2133 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2133 Speed Bin							-093E		-093		
CL-*n*RCD-*n*RP							15-15-15		16-16-16		
Parameter						Symbol	Min	Max	Min	Max	Unit
Internal READ command to first data						^{t}AA	14.06 (13.50)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						^{t}AA_DBI	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time						^{t}RCD	14.06 (13.50)[4]	–	15.00	–	ns
PRECHARGE command period						^{t}RP	14.06 (13.50)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	33	9 × ^{t}REFI	33	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns): non-DBI**	**READ CL: non-DBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	–	13.50	9	11	9	^{t}CK (AVG)	1.500	1.900[6]	Reserved		ns
	–	15.00	10	12		^{t}CK (AVG)	1.500[6]	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)			1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^{t}CK (AVG)	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^{t}CK (AVG)			1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^{t}CK (AVG)	0.937	<1.071	Reserved		ns
	-093	15.00	16	19		^{t}CK (AVG)			0.937	<1.071	ns
Supported CL settings							9, 10[6], 11–16		10, 12, 14, 16		*n*CK
Supported CL settings with read DBI							11, 12[6], 13–16, 18-19		12, 14, 16, 19		*n*CK
Supported CWL settings							9, 10, 11, 12, 14		9, 10, 11, 12, 14		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.

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2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 161: DDR4-2400 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2400 Speed Bin							-083E		-083		-083D		Unit
CL-*n*RCD-*n*RP							16-16-16		17-17-17		18-18-18		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	
Internal READ command to first data						^{t}AA	13.32	19.00[6]	14.16 (13.75)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						$^{t}AA\_DBI$	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time						^{t}RCD	13.32	–	14.16 (13.75)[4]	–	15.00	19.00	ns
PRECHARGE command period						^{t}RP	13.32	–	14.16 (13.75)[4]	–	15.00	19.00	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	32	9 × $^{t}REFI$	32	9 × $^{t}REFI$	32	9 × $^{t}REFI$	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**$^{t}AAmin$ (ns): non-DBI**	**READ CL: non-DBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	–	13.50	9	11	9	^{t}CK (AVG)	1.500	1.900[6]	Reserved		Reserved		ns
	–	15.00	10	12		^{t}CK (AVG)	1.500[6]	1.900[6]	1.500	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)					1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^{t}CK (AVG)	1.071	<1.250	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^{t}CK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^{t}CK (AVG)	0.937	<1.071	0.937	<1.071	Reserved		ns
	-093	15.00	16	19		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	^{t}CK (AVG)	0.833	<0.937	Reserved		Reserved		ns
	-083	14.16	17	20		^{t}CK (AVG)			0.833	<0.937			ns
	-083D	15.00	18	21		^{t}CK (AVG)					0.833	<0.937	ns

DDR4-2400 Speed Bin		-083E		-083		-083D		
CL-*n*RCD-*n*RP		16-16-16		17-17-17		18-18-18		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Supported CL settings		9, 10[6], 11–18		10–18		10, 12, 14, 16, 18		*n*CK
Supported CL settings with read DBI		11, 12[6], 13–16, 18–21		12–16, 18–21		12, 14, 16, 19, 21		*n*CK
Supported CWL settings		9–12, 14, 16		9-12, 14, 16		9–12, 14, 16		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2[t]CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable [t]CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native [t]CK-CL-*n*RCD-*n*RP combinations.
5. When calculating [t]RC in clocks, values may not be used in a combination that violate [t]RAS or [t]RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 162: DDR4-2666 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2666 Speed Bin							-075E		-075		-075D		Unit
CL-*n*RCD-*n*RP							18-18-18		19-19-19		20-20-20		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	
Internal READ command to first data						^{t}AA	13.50	19.00[6]	14.25 (13.75)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						$^{t}AA\_DBI$	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	^{t}AA (MIN) + 3*n*CK	^{t}AA (MAX) + 3*n*CK	ns
ACTIVATE to internal READ or WRITE delay time						^{t}RCD	13.50	–	14.25 (13.75)[4]	–	15.00	–	ns
PRECHARGE command period						^{t}RP	13.50	–	14.25 (13.75)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	32	9 × $^{t}REFI$	32	9 × $^{t}REFI$	32	9 × $^{t}REFI$	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**$^{t}AAmin$ (ns): non-DBI**	**READ CL: non-DBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	-	13.50	9	11	9	^{t}CK (AVG)	1.500	1.900[6]	Reserved		Reserved		ns
	-	15.00	10	12		^{t}CK (AVG)			1.500	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)					1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^{t}CK (AVG)	1.071	<1.250	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^{t}CK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^{t}CK (AVG)	0.937	<1.071	0.937	<1.071	Reserved		ns
	-093	15.00	16	19		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-083	14.16	17	20		^{t}CK (AVG)	0.833	<0.937	0.833	<0.937			ns
	-083D	15.00	18	21		^{t}CK (AVG)					0.833	<0.937	ns

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DDR4-2666 Speed Bin							-075E		-075		-075D		
CL-*n*RCD-*n*RP							18-18-18		19-19-19		20-20-20		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
2666	-075E	13.50	18	21	14, 18	^{t}CK (AVG)	0.750	<0.833	Reserved		Reserved		ns
	-075	14.25	19	22		^{t}CK (AVG)			0.750	<0.833			ns
	-075D	15.00	20	23		^{t}CK (AVG)					0.750	<0.833	ns
Supported CL settings							9–20		10-20		10, 12, 14, 16, 18, 20		*n*CK
Supported CL settings with read DBI							11–16, 18–23		12–16, 18–23		12, 14, 16, 19, 21, 23		*n*CK
Supported CWL settings							9–12, 14, 16, 18		9–12, 14, 16, 18		9–12, 14, 16, 18		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 163: DDR4-2933 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2933 Speed Bin							-068E		-068		-068D		Unit
CL-*n*RCD-*n*RP							20-20-20		21-21-21		22-22-22		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	
Internal READ command to first data						^{t}AA	13.64	19.00[6]	14.32 (13.75)[4]	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						^{t}AA_DBI	^{t}AA (MIN) + 4*n*CK	^{t}AA (MAX) + 4*n*CK	^{t}AA (MIN) + 4*n*CK	^{t}AA (MAX) + 4*n*CK	^{t}AA (MIN) + 4*n*CK	^{t}AA (MAX) + 4*n*CK	ns
ACTIVATE-to-internal READ or WRITE delay time						^{t}RCD	13.64	–	14.32 (13.75)[4]	–	15.00	–	ns
PRECHARGE command period						^{t}RP	13.64	–	14.32 (13.75)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^{t}RAS	32	9 × ^{t}REFI	32	9 × ^{t}REFI	32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin(ns): non-DBI**	**READ CL: non-DBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	–	13.50	9	11	9	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	–	15.00	10	12		^{t}CK (AVG)	1.500	1.900[6]	1.500	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^{t}CK (AVG)	1.250	<1.500	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^{t}CK (AVG)					1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^{t}CK (AVG)	1.071	<1.250	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^{t}CK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^{t}CK (AVG)	0.937	<1.071	0.937	<1.071	Reserved		ns
	-093	15.00	16	19		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083E	13.32	16	19	12, 16	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-083	14.16	17	20		^{t}CK (AVG)	0.833	<0.937	0.833	<0.937			ns
	083D	15.00	18	21		^{t}CK (AVG)					0.833	<0.937	ns

DDR4-2933 Speed Bin							-068E		-068		-068D		
CL-*n*RCD-*n*RP							20-20-20		21-21-21		22-22-22		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
2666	-075E	13.50	18	21	14, 18	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-075	14.25	19	22		^{t}CK (AVG)	0.750	<0.833	0.750	<0.833			ns
	-075D	15.00	20	23		^{t}CK (AVG)					0.750	<0.833	ns
2933	-068E	13.64	20	24	16, 20	^{t}CK (AVG)	0.682	<0.750	Reserved		Reserved		ns
	-068	14.32	21	25		^{t}CK (AVG)			0.682	<0.750			ns
	-068D	15.00	22	26		^{t}CK (AVG)					0.682	<0.750	ns
	–	16.37	24	28		^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
Supported CL settings							10–22		10–22		10, 12, 14, 16, 18, 20, 22		*n*CK
Supported CL settings with read DBI							12–16, 18–26		12–16,18–23, 25-26		12, 14, 16, 19, 21, 23, 26		*n*CK
Supported CWL settings							9–12, 14, 16, 18, 20		9–12, 14, 16, 18, 20		9–12, 14, 16, 18, 20		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 164: DDR4-3200 Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-3200 Speed Bin							-062Y[6]		-062E		-062		
CL-*n*RCD-*n*RP							22-22-22		22-22-22		24-24-24		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data						^tAA	13.75 (13.32)[4]	19.00[6]	13.75	19.00[6]	15.00	19.00[6]	ns
Internal READ command to first data with read DBI enabled						^tAA_DBI	^tAA (MIN) + 4*n*CK	^tAA (MAX) + 4*n*CK	^tAA (MIN) + 4*n*CK	^tAA (MAX) + 4*n*CK	^tAA (MIN) + 4*n*CK	^tAA (MAX) + 4*n*CK	ns
ACTIVATE-to-internal READ or WRITE delay time						^tRCD	13.75 (13.32)[4]	–	13.75	–	15.00	–	ns
PRECHARGE command period						^tRP	13.75 (13.32)[4]	–	13.75	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period						^tRAS	32	9 × ^tREFI	32	9 × ^tREFI	32	9 × ^tREFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period						^tRC[5]	^tRAS + ^tRP	–	^tRAS + ^tRP	–	^tRAS + ^tRP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^tAAmin (ns): non-DBI**	**READ CL: non-DBI**	**READ CL: DBI**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1333	-	13.50	9	11	9	^tCK (AVG)	1.500	1.900[6]	Reserved		Reserved		ns
	-	15.00	10	12		^tCK (AVG)			1.500	1.900[6]	1.500	1.900[6]	ns
1600	-125E	13.75	11	13	9, 11	^tCK (AVG)	1.250	<1.500	1.250	<1.500	Reserved		ns
	-125	15.00	12	14		^tCK (AVG)					1.250	<1.500	ns
1866	-107E	13.92	13	15	10, 12	^tCK (AVG)	1.071	<1.250	1.071	<1.250	Reserved		ns
	-107	15.00	14	16		^tCK (AVG)					1.071	<1.250	ns
2133	-093E	14.06	15	18	11, 14	^tCK (AVG)	0.937	<1.071	0.937	<1.071	Reserved		ns
	-093	15.00	16	19		^tCK (AVG)					0.937	<1.071	ns

DDR4-3200 Speed Bin							-062Y[6]		-062E		-062		
CL-*n*RCD-*n*RP							22-22-22		22-22-22		24-24-24		
Parameter						Symbol	Min	Max	Min	Max	Min	Max	Unit
2400	-083E	13.32	16	19	12, 16	^{t}CK (AVG)	0.833	<0.937	Reserved		Reserved		ns
	-083	14.16	17	20		^{t}CK (AVG)			0.833	<0.937			ns
	-083D	15.00	18	21		^{t}CK (AVG)					0.833	<0.937	ns
2666	-075E	13.50	18	21	14, 18	^{t}CK (AVG)	0.750	<0.833	Reserved		Reserved		ns
	-075	14.25	19	22		^{t}CK (AVG)			0.750	<0.833			ns
	-075D	15.00	20	23		^{t}CK (AVG)					0.750	<0.833	ns
2933	-068E	13.64	20	24	16, 20	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-068	14.32	21	25		^{t}CK (AVG)	0.682	<0.750	0.682	<0.750			ns
	-068D	15.00	22	26		^{t}CK (AVG)			0.682	<0.750	0.682	<0.750	ns
	–	16.37	24	28		^{t}CK (AVG)					0.682	<0.750	ns
3200	-062E	13.75	22	26	16, 20	^{t}CK (AVG)	0.625	<0.682	0.625	<0.682	Reserved		ns
	-062	15.00	24	28		^{t}CK (AVG)					0.625	<0.682	ns
Supported CL settings							9–22, 24		10–22, 24		10, 12, 14, 16, 18, 20, 22, 24		*n*CK
Supported CL settings with read DBI							11–16, 18–23, 25-26, 28		12–16, 18–23, 25-26, 28		12, 14, 16, 19, 21, 23, 26, 28		*n*CK
Supported CWL settings							9–12, 14, 16, 18, 20		9–12, 14, 16, 18, 20		9–12, 14, 16, 18, 20		*n*CK

Notes: 1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Refresh Parameters By Device Density

Table 165: Refresh Parameters by Device Density

Parameter	Symbol		2Gb	4Gb	8Gb	16Gb	Unit	Notes
REF command to ACT or REF command time	^{t}RFC (All bank groups)		160	260	350	350	ns	
Average periodic refresh interval	^{t}REFI	-40°C ≤ T_C ≤ 85°C	7.8	7.8	7.8	7.8	µs	
		85°C < T_C ≤ 95°C	3.9	3.9	3.9	3.9	µs	1
		95°C < T_C ≤ 105°C	1.95	1.95	1.95	1.95	µs	1

Notes: 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

AC Electrical Characteristics and AC Timing Parameters

Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average (DLL off mode)		^{t}CK (AVG, DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Clock period average		^{t}CK (AVG, DLL_ON)	1.25	1.9	1.071	1.9	0.937	1.9	0.833	1.9	ns	3 , 13
High pulse width average		^{t}CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK (AVG)	
Low pulse width average		^{t}CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK (AVG)	
Clock period jitter	Total	^{t}JITper_tot	–63	63	–54	54	–47	47	–42	42	ps	17 , 18
	Deterministic	^{t}JITper_dj	–31	31	–27	27	–23	23	–21	21	ps	17
	DLL locking	^{t}JITper,lck	–50	50	–43	43	–38	38	-33	33	ps	
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper_tot MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper_tot MAX								ps	
Clock absolute high pulse width (includes duty cycle jitter)		^{t}CH (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Clock absolute low pulse width (includes duty cycle jitter)		^{t}CL (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Cycle-to-cycle jitter	Total	^{t}JITcc _tot	–	125	–	107	–	94	–	83	ps	
	DLL locking	^{t}JITcc,lck	–	100	–	86	–	75	–	67	ps	

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across	2 cycles	^{t}ERR2per	–92	92	–79	79	–69	69	–61	61	ps	
	3 cycles	^{t}ERR3per	–109	109	–94	94	–82	82	–73	73	ps	
	4 cycles	^{t}ERR4per	–121	121	–104	104	–91	91	–81	81	ps	
	5 cycles	^{t}ERR5per	–131	131	–112	112	–98	98	–87	87	ps	
	6 cycles	^{t}ERR6per	–139	139	–119	119	–104	104	–92	92	ps	
	7 cycles	^{t}ERR7per	–145	145	–124	124	–109	109	–97	97	ps	
	8 cycles	^{t}ERR8per	–151	151	–129	129	–113	113	–101	101	ps	
	9 cycles	^{t}ERR9per	–156	156	–134	134	–117	117	–104	104	ps	
	10 cycles	^{t}ERR10per	–160	160	–137	137	–120	120	–107	107	ps	
	11 cycles	^{t}ERR11per	–164	164	–141	141	–123	123	–110	110	ps	
	12 cycles	^{t}ERR12per	–168	168	–144	144	–126	126	–112	112	ps	
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper_tot MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper_tot MAX								ps	
DQ Input Timing												
Data setup time to DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DS	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Noncalibrated V_{REF}	^{t}PDA_S	minimum of 0.5UI								UI	22
Data hold time from DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DH	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Noncalibrated V_{REF}	^{t}PDA_H	minimum of 0.5UI								UI	22
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	–	0.58	–	0.58	–	0.58	–	UI	
DQ Output Timing (DLL enabled)												
DQS_t, DQS_c to DQ skew, per group, per access		^{t}DQSQ	–	0.16	–	0.16	–	0.16	–	0.17	UI	
DQ output hold time from DQS_t, DQS_c		^{t}QH	0.76	–	0.76	–	0.76	–	0.74	–	UI	

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Valid Window per device: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{d}$	0.63		0.63		0.64		0.64		UI	
Data Valid Window per device, per pin: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{p}$	0.66	–	0.66	–	0.69	–	0.72	–	UI	
DQ Low-Z time from CK_t, CK_c	^{t}LZDQ	–450	225	–390	195	–360	180	–330	175	ps	
DQ High-Z time from CK_t, CK_c	^{t}HZDQ	–	225	–	195	–	180	–	175	ps	
DQ Strobe Input Timing											
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DQSS_{1ck}$	–0.27	0.27	–0.27	0.27	–0.27	0.27	–0.27	0.27	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DQSS_{2ck}$	NA		NA		NA		–0.50	0.50	CK	
DQS_t, DQS_c differential input low pulse width	^{t}DQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width	^{t}DQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width for 2^{t}CK preamble	^{t}DQSH2PRE	NA		NA		NA		1.46	-	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSS_{1ck}$	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSS_{2ck}$	NA		NA		NA		0	-	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSH_{1ck}$	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSH_{2ck}$	NA		NA		NA		0	-	CK	
DQS_t, DQS_c differential WRITE preamble for 1^{t}CK preamble	$^{t}WPRE_{1ck}$	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential WRITE preamble for 2^{t}CK preamble	$^{t}WPRE_{2ck}$	NA		NA		NA		1.8	–	CK	
DQS_t, DQS_c differential WRITE postamble	^{t}WPST	0.33	–	0.33	–	0.33	–	0.33	–	CK	
DQS Strobe Output Timing (DLL enabled)											

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c		^{t}DQSCK	–225	225	–195	195	–180	180	–175	175	ps	
DQS_t, DQS_c rising edge output variance window per DRAM		^{t}DQSCKi	–	370	–	330	–	310	–	290	ps	
DQS_t, DQS_c differential output high time		^{t}QSH	0.4	–	0.4	–	0.4	–	0.4	–	CK	
DQS_t, DQS_c differential output low time		^{t}QSL	0.4	–	0.4	–	0.4	–	0.4	–	CK	
DQS_t, DQS_c Low-Z time (RL - 1)		^{t}LZDQS	–450	225	–390	195	–360	180	–330	175	ps	
DQS_t, DQS_c High-Z time (RL + BL/2)		^{t}HZDQS	–	225	–	195	–	180	–	175	ps	
DQS_t, DQS_c differential READ preamble for 1^{t}CK preamble		^{t}RPRE$_{1ck}$	0.9	–	0.9	–	0.9	–	0.9	–	CK	20
DQS_t, DQS_c differential READ preamble for 2^{t}CK preamble		^{t}RPRE$_{2ck}$	NA		NA		NA		1.8	–	CK	20
DQS_t, DQS_c differential READ postamble		^{t}RPST	0.33	–	0.33	–	0.33	–	0.33	–	CK	21
Command and Address Timing												
DLL locking time		^{t}DLLK	597	–	597	–	768	–	768	–	CK	2, 4
CMD, ADDR setup time to CK_t, CK_c Base referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^{t}IS	115	–	100	–	80	–	62	–	ps	
	V_{REFCA}	^{t}IS$_{VREF}$	215	–	200	–	180	–	162	–	ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^{t}IH	140	–	125	–	105	–	87	–	ps	
	V_{REFCA}	^{t}IH$_{VREF}$	215	–	200	–	180	–	162	–	ps	
CTRL, ADDR pulse width for each input		^{t}IPW	600	–	525	–	460	–	410	–	ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD								ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP								ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS								ns	12
ACTIVATE-to-ACTIVATE or REF command period		^{t}RC	See Speed Bin Tables for ^{t}RC								ns	12
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size		^{t}RRD_S (1/2KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK	1

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size	$^{t}RRD\_S$ (1KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size	$^{t}RRD\_S$ (2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size	$^{t}RRD\_L$ (1/2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size	$^{t}RRD\_L$ (1KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size	$^{t}RRD\_L$ (2KB)	MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		CK	1
Four ACTIVATE windows for 1/2KB page size	^{t}FAW (1/2KB)	MIN = greater of 16CK or 20ns		MIN = greater of 16CK or 17ns		MIN = greater of 16CK or 15ns		MIN = greater of 16CK or 13ns		ns	
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN = greater of 20CK or 25ns		MIN = greater of 20CK or 23ns		MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns		ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN = greater of 28CK or 35ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		ns	
WRITE recovery time	$^{t}WR_{1ck}$	MIN = 15ns								ns	1, 5, 9
	$^{t}WR_{2ck}$	MIN = 1CK + $^{t}WR_{1ck}$								CK	1, 5, 10
WRITE recovery time when CRC and DM are both enabled	$^{t}WR\_CRC\_DM_{1ck}$	MIN = $^{t}WR_{1ck}$ + greater of (4CK or 3.75ns)		MIN = $^{t}WR_{1ck}$ + greater of (5CK or 3.75ns)						CK	1, 6, 9
	$^{t}WR\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WR\_CRC\_DM_{1ck}$								CK	1, 6, 10
Delay from start of internal WRITE transaction to internal READ command – Same bank group	$^{t}WTR\_L_{1ck}$	MIN = greater of 4CK or 7.5ns								CK	1, 5, 9
	$^{t}WTR\_L_{2ck}$	MIN = 1CK + $^{t}WTR\_L_{1ck}$								CK	1, 5, 10
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	$^{t}WTR\_L\_CRC\_DM_{1ck}$	MIN = $^{t}WTR\_L_{1ck}$ + greater of (4CK or 3.75ns)		MIN = $^{t}WTR\_L_{1ck}$ + greater of (5CK or 3.75ns)						CK	1, 6, 9
	$^{t}WTR\_L\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WTR\_L\_CRC\_DM_{1ck}$								CK	1, 6, 10

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Delay from start of internal WRITE transaction to internal READ command – Different bank group	$^{t}WTR\_S_{1ck}$	MIN = greater of (2CK or 2.5ns)								CK	1, 5, 7, 8, 9
	$^{t}WTR\_S_{2ck}$	MIN = 1CK + $^{t}WTR\_S_{1ck}$								CK	1, 5, 7, 8, 10
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	$^{t}WTR\_S\_CRC\_DM_{1ck}$	MIN = $^{t}WTR\_S_{1ck}$ + greater of (4CK or 3.75ns)		MIN = $^{t}WTR\_S_{1ck}$ + greater of (5CK or 3.75ns)						CK	1, 6, 7, 8, 9
	$^{t}WTR\_S\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WTR\_S\_CRC\_DM_{1ck}$								CK	1, 6, 7, 8, 10
READ-to-PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns								CK	1
CAS_n-to-CAS_n command delay to different bank group	$^{t}CCD\_S$	4	–	4	–	4	–	4	–	CK	
CAS_n-to-CAS_n command delay to same bank group	$^{t}CCD\_L$	MIN = greater of 4CK or 6.25ns	–	MIN = greater of 4CK or 5.355ns	–	MIN = greater of 4CK or 5.355ns	–	MIN = greater of 4CK or 5ns	–	CK	14
Auto precharge write recovery + precharge time	^{t}DAL (MIN)	MIN = WR + ROUND$^{t}RP/^{t}CK$ (AVG); MAX = N/A								CK	8
MRS Command Timing											
MRS command cycle time	^{t}MRD	8	–	8	–	8	–	8	–	CK	
MRS command cycle time in PDA mode	$^{t}MRD\_PDA$	MIN = greater of (16nCK, 10ns)								CK	1
MRS command cycle time in CAL mode	$^{t}MRD\_CAL$	MIN = ^{t}MOD + ^{t}CAL								CK	
MRS command update delay	^{t}MOD	MIN = greater of (24nCK, 15ns)								CK	1
MRS command update delay in PDA mode	$^{t}MOD\_PDA$	MIN = ^{t}MOD								CK	
MRS command update delay in CAL mode	$^{t}MOD\_CAL$	MIN = ^{t}MOD + ^{t}CAL								CK	
MRS command to DQS drive in preamble training	^{t}SDO	MIN = ^{t}MOD + 9ns									
MPR Command Timing											
Multipurpose register recovery time	$^{t}MPRR$	MIN = 1CK								CK	

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Multipurpose register write recovery time	^{t}WR_MPR	MIN = ^{t}MOD + AL + PL									
CRC Error Reporting Timing											
CRC error to ALERT_n latency	^{t}CRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	^{t}CRC_ALERT_PW	6	10	6	10	6	10	6	10	CK	
CA Parity Timing											
Parity latency	PL	4	–	4	–	4	–	5	–	CK	
Commands uncertain to be executed during this time	^{t}PAR_UNKNOWN	–	PL	–	PL	–	PL	–	PL	CK	
Delay from errant command to ALERT_n assertion	^{t}PAR_ALERT_ON	–	PL + 6ns	–	P L + 6ns	–	PL + 6ns	–	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	^{t}PAR_ALERT_PW	48	96	56	112	64	128	72	144	CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^{t}PAR_ALERT_RSP	–	43	–	50	–	57	–	64	CK	
CAL Timing											
CS_n to command address latency	^{t}CAL	3	–	4	–	4	–	5	–	CK	19
CS_n to command address latency in gear-down mode	^{t}CALg	N/A	–	N/A	–	N/A	–	N/A	–	CK	
MPSM Timing											
Command path disable delay upopn MPSM entry	^{t}MPED	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)								CK	1
Valid clock requirement after MPSM entry	^{t}CKMPE	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)								CK	1
Valid clock requirement before MPSM exit	^{t}CKMPX	MIN = ^{t}CKSRX (MIN)								CK	1
Exit MPSM to commands not requiring a locked DLL	^{t}XMP	^{t}XS (MIN)								CK	
Exit MPSM to commands requiring a locked DLL	^{t}XMPDLL	MIN = ^{t}XMP (MIN) + ^{t}XSDLL (MIN)								CK	1
CS setup time to CKE	^{t}MPX_S	MIN = ^{t}IS (MIN) + ^{t}IH (MIN)								ns	
CS_n HIGH hold time to CKE rising edge	^{t}MPX_HH	MIN = ^{t}XP								ns	

Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
CS_n LOW hold time to CKE rising edge		^{t}MPX_LH	12	^{t}XMP-10ns	12	^{t}XMP-10ns	12	^{t}XMP-10ns	12	^{t}XMP-10ns	ns	
Connectivity Test Timing												
TEN pin HIGH to CS_n LOW – Enter CT mode		^{t}CT_Enable	200	–	200	–	200	–	200	–	ns	
CS_n LOW and valid input to valid output		^{t}CT_Valid	–	200	–	200	–	200	–	200	ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		^{t}CTCKE_Valid	10	–	10	–	10	–	10	–	ns	
Calibration and V_{REFDQ} Train Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	1024	–	1024	–	1024	–	1024	–	CK	
	Normal operation	^{t}ZQoper	512	–	512	–	512	–	512	–	CK	
ZQCS command: Short calibration time		^{t}ZQCS	128	–	128	–	128	–	128	–	CK	
The V_{REF} increment/decrement step time		V_{REF_time}	MIN = 150ns									
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		^{t}VREFDQE	MIN = 150ns								ns	1
Exit V_{REFDQ} training mode to the first WRITE command delay		^{t}VREFDQX	MIN = 150ns								ns	1
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = ^{t}RFC1 + 10ns								ns	1
RESET_L pulse low after power stable		^{t}PW_RESET_S	1.0	–	1.0	–	1.0	–	1.0	–	µs	
RESET_L pulse low at power-up		^{t}PW_RESET_L	200	–	200	–	200	–	200	–	µs	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200								ms	
RESET_n LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 0								ns	
Refresh Timing												

Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	^{t}RFC1	MIN = 260								ns	1, 11
		^{t}RFC2	MIN = 160								ns	1, 11
		^{t}RFC4	MIN = 110								ns	1, 11
	8Gb	^{t}RFC1	MIN = 350								ns	1, 11
		^{t}RFC2	MIN = 260								ns	1, 11
		^{t}RFC4	MIN = 160								ns	1, 11
	16Gb	^{t}RFC1	MIN = 350								ns	1, 11
		^{t}RFC2	MIN = 260								ns	1, 11
		^{t}RFC4	MIN = 160								ns	1, 11
Average periodic refresh interval	-40°C ≤ T_C ≤ 85°C	^{t}REFI	MIN = N/A; MAX = 7.8								µs	11
	85°C < T_C ≤ 95°C	^{t}REFI	MIN = N/A; MAX = 3.9								µs	11
	95°C < T_C ≤ 105°C	^{t}REFI	MIN = N/A; MAX = 1.95								µs	11
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = ^{t}RFC1 + 10ns								ns	1
Exit self refresh to commands not requiring a locked DLL in self refresh abort		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)		^{t}XS_FAST	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN)								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + 1*n*CK								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled		^{t}CKESR_PAR	MIN = ^{t}CKE (MIN) + 1*n*CK + PL								CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)		^{t}CKSRE	MIN = greater of (5CK, 10ns)								CK	1

Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Valid clock requirement after self refresh entry or power-down when CA parity is enabled	^{t}CKSRE_PAR	MIN = greater of (5CK, 10ns) + PL								CK	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	^{t}CKSRX	MIN = greater of (5CK, 10ns)								CK	1
Power-Down Timing											
Exit power-down with DLL on to any valid command	^{t}XP	MIN = greater of 4CK or 6ns								CK	1
Exit power-down with DLL on to any valid command when CA Parity is enabled.	^{t}XP _PAR	MIN = (greater of 4CK or 6ns) + PL								CK	1
CKE MIN pulse width	^{t}CKE (MIN)	MIN = greater of 3CK or 5ns								CK	1
Command pass disable delay	^{t}CPDED	4	–	4	–	4	–	4	–	CK	
Power-down entry to power-down exit timing	^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI								CK	
Begin power-down period prior to CKE registered HIGH	^{t}ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	^{t}ANPD + ^{t}XSDLL								CK	
Power-Down Entry Minimum Timing											
ACTIVATE command to power-down entry	^{t}ACTPDEN	1	–	1	–	2	–	2	–	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	^{t}PRPDEN	1	–	1	–	2	–	2	–	CK	
REFRESH command to power-down entry	^{t}REFPDEN	1	–	1	–	2	–	2	–	CK	
MRS command to power-down entry	^{t}MRSPDEN	MIN = ^{t}MOD (MIN)								CK	1
READ/READ with auto precharge command to power-down entry	^{t}RDPDEN	MIN = RL + 4 + 1								CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)								CK	1
WRITE command to power-down entry (BC4MRS)	^{t}WRPBC4DEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)								CK	1

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Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	^{t}WRAPDEN	MIN = WL + 4 + WR + 1								CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	^{t}WRAPBC4DEN	MIN = WL + 2 + WR + 1								CK	1
ODT Timing											
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2								CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2								CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	^{t}AONAS	1	9	1	9	1	9	1	9	ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	^{t}AOFAS	1	9	1	9	1	9	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1^{t}CK	6	–	6	–	6	–	6	–	CK	
	ODTH8 2^{t}CK	NA		NA		NA		7	–		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1^{t}CK	4	–	4	–	4	–	4	–	CK	
	ODTH4 2^{t}CK	NA		NA		NA		5	–		
Write Leveling Timing											
First DQS_t, DQS_c rising edge after write leveling mode is programmed	^{t}WLMRD	40	–	40	–	40	–	40	–	CK	
DQS_t, DQS_c delay after write leveling mode is programmed	^{t}WLDQSEN	25	–	25	–	25	–	25	–	CK	
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	^{t}WLS	0.13	–	0.13	–	0.13	–	0.13	–	^{t}CK (AVG)	
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	^{t}WLH	0.13	–	0.13	–	0.13	–	0.13	–	^{t}CK (AVG)	
Write leveling output delay	^{t}WLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	0	2	0	2	ns	
Gear-Down Timing (Not Supported Below DDR4-2666)											
Exit reset from CKE HIGH to a valid MRS gear-down	^{t}XPR_GEAR	N/A		N/A		N/A		N/A		CK	

Table 166: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CKE HIGH assert to gear-down enable time)	^{t}XS_GEAR	N/A		N/A		N/A		N/A		CK	
MRS command to sync pulse time	^{t}SYNC_GEAR	N/A		N/A		N/A		N/A		CK	
Sync pulse to first valid command	^{t}CMD_GEAR	N/A		N/A		N/A		N/A		CK	
Gear-down setup time	^{t}GEAR_setup	N/A	–	N/A	–	N/A	–	N/A	–	CK	
Gear-down hold time	^{t}GEAR_hold	N/A	–	N/A	–	N/A	–	N/A	–	CK	

Notes:
1. Maximum limit not applicable.
2. Micron tDLLK values support the legacy JEDEC tDLLK specifications.
3. DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.
4. Data rate is greater than or equal to 1066 Mb/s.
5. WRITE-to-READ when CRC and DM are both not enabled.
6. WRITE-to-READ delay when CRC and DM are both enabled.
7. The start of internal write transactions is defined as follows:
   - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
8. For these parameters, the device supports ^{t}nPARAM [nCK] = ROUND{^{t}PARAM [ns]/^{t}CK (AVG) [ns]} according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.
9. When operating in 1^{t}CK WRITE preamble mode.
10. When operating in 2^{t}CK WRITE preamble mode.
11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to ^{t}RFC refresh time.
12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
13. Applicable from ^{t}CK (AVG) MIN to ^{t}CK (AVG) MAX as stated in the Speed Bin tables.
14. JEDEC specifies a minimum of five clocks.
15. The maximum read postamble is bound by ^{t}DQSCK (MIN) plus ^{t}QSH (MIN) on the left side and ^{t}HZ(DQS) MAX on the right side.
16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately 0.7 × V_{DDQ} as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to V_{TT} = V_{DDQ}.
17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.
19. The actual ^{t}CAL minimum is the larger of 3 clocks or 3.748ns/^{t}CK; the table lists the applicable clocks required at targeted speed bin.

20. The maximum READ preamble is bounded by ^{t}LZ(DQS) MIN on the left side and ^{t}DQSCK (MAX) on the right side. See figure in the Clock to Data Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2^{t}CK toggle mode, as illustrated in the READ Preamble section.
21. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
22. The ^{t}PDA_S/^{t}PDA_H parameters may use the ^{t}DS/^{t}DH limits, respectively, if the signal is LOW the entire BL8.

Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

Table 167: Electrical Characteristics and AC Timing Parameters

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average (DLL off mode)		^{t}CK (AVG, DLL_OFF)	8	20	8	20	8	20			ns	
Clock period average		^{t}CK (AVG, DLL_ON)	0.75	1.9	0.682	1.9	0.625	1.9			ns	3, 13
High pulse width average		^{t}CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			^{t}CK (AVG)	
Low pulse width average		^{t}CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			^{t}CK (AVG)	
Clock period jitter	Total	^{t}JITper_tot	–38	38	-34	34	–32	32			ps	17 , 18
	Deterministic	^{t}JITper_dj	–19	19	-17	17	–16	16			ps	17
	DLL locking	^{t}JITper,lck	–30	30	-27	27	–25	25			ps	
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper_tot MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper_tot MAX								ps	
Clock absolute high pulse width (includes duty cycle jitter)		^{t}CH (ABS)	0.45	–	0.45	–	0.45	–			^{t}CK (AVG)	
Clock absolute low pulse width (includes duty cycle jitter)		^{t}CL (ABS)	0.45	–	0.45	–	0.45	–			^{t}CK (AVG)	
Cycle-to-cycle jitter	Total	^{t}JITcc _tot	–	75	–	68	–	62			ps	
	DLL locking	^{t}JITcc,lck	–	60	–	55	–	62			ps	

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across	2 cycles	^{t}ERR2per	–55	55	-50	50	–46	46			ps	
	3 cycles	^{t}ERR3per	–66	66	-60	60	–55	55			ps	
	4 cycles	^{t}ERR4per	–73	73	-66	66	–61	61			ps	
	5 cycles	^{t}ERR5per	–78	78	-71	71	–65	65			ps	
	6 cycles	^{t}ERR6per	–83	83	-75	75	–69	69			ps	
	7 cycles	^{t}ERR7per	–87	87	-79	79	–73	73			ps	
	8 cycles	^{t}ERR8per	–91	91	-83	83	–76	76			ps	
	9 cycles	^{t}ERR9per	–94	94	-85	85	–78	78			ps	
	10 cycles	^{t}ERR10per	–96	96	-88	88	–80	80			ps	
	11 cycles	^{t}ERR11per	–99	99	-90	90	–83	83			ps	
	12 cycles	^{t}ERR12per	–101	101	-92	92	–84	84			ps	
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper_tot MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper_tot MAX								ps	
DQ Input Timing												
Data setup time to DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DS	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Non-calibrated V_{REF}	^{t}PDA_S	minimum of 0.5ui								UI	22
Data hold time from DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DH	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Non-calibrated V_{REF}	^{t}PDA_H	minimum of 0.5UI								UI	22
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	–	0.58	–	0.58	–			UI	
DQ Output Timing (DLL enabled)												
DQS_t, DQS_c to DQ skew, per group, per access		^{t}DQSQ	–	0.18	–	0.19	–	0.20			UI	
DQ output hold time from DQS_t, DQS_c		^{t}QH	0.74	–	0.72	–	0.70	–			UI	

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Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Valid Window per device: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{d}$	0.64	–	0.64	–	0.64	–			UI	
Data Valid Window per device, per pin: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{p}$	0.72	–	0.72	–	0.72	–			UI	
DQ Low-Z time from CK_t, CK_c	^{t}LZDQ	–310	170	–280	165	–250	160			ps	
DQ High-Z time from CK_t, CK_c	^{t}HZDQ	–	170	–	165	–	160			ps	
DQ Strobe Input Timing											
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DQSS_{1ck}$	–0.27	0.27	–0.27	0.27	–0.27	0.27			CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DQSS_{2ck}$	–0.50	0.50	–0.50	0.50	–0.50	0.50			CK	
DQS_t, DQS_c differential input low pulse width	^{t}DQSL	0.46	0.54	0.46	0.54	0.46	0.54			CK	
DQS_t, DQS_c differential input high pulse width	^{t}DQSH	0.46	0.54	0.46	0.54	0.46	0.54			CK	
DQS_t, DQS_c differential input high pulse width for 2^{t}CK preamble	^{t}DQSH2PRE	1.46	-	1.46	-	1.46	-			CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSS_{1ck}$	0.18	–	0.18	–	0.18	–			CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSS_{2ck}$	0	–	0	–	0	–			CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSH_{1ck}$	0.18	–	0.18	–	0.18	–			CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSH_{2ck}$	0	–	0	–	0	–			CK	
DQS_t, DQS_c differential WRITE preamble for 1^{t}CK preamble	$^{t}WPRE_{1ck}$	0.9	–	0.9	–	0.9	–			CK	
DQS_t, DQS_c differential WRITE preamble for 2^{t}CK preamble	$^{t}WPRE_{2ck}$	1.8	–	1.8	–	1.8	–			CK	
DQS_t, DQS_c differential WRITE postamble	^{t}WPST	0.33	–	0.33	–	0.33	–			CK	

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS Strobe Output Timing (DLL enabled)												
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c		^{t}DQSCK	–170	170	–165	165	–160	160			ps	
DQS_t, DQS_c rising edge output variance window per DRAM		^{t}DQSCKi	–	270	–	265	–	260			ps	
DQS_t, DQS_c differential output high time		^{t}QSH	0.40	–	0.40	–	0.40	–			CK	
DQS_t, DQS_c differential output low time		^{t}QSL	0.40	–	0.40	–	0.40	–			CK	
DQS_t, DQS_c Low-Z time (RL - 1)		^{t}LZDQS	–310	170	–280	165	–250	160			ps	
DQS_t, DQS_c High-Z time (RL + BL/2)		^{t}HZDQS	–	170	–	165	–	160			ps	
DQS_t, DQS_c differential READ preamble for 1^{t}CK preamble		$^{t}RPRE_{1ck}$	0.9	–	0.9	–	0.9	–			CK	20
DQS_t, DQS_c differential READ preamble for 2^{t}CK preamble		$^{t}RPRE_{2ck}$	1.8	–	1.8	–	1.8	–			CK	20
DQS_t, DQS_c differential READ postamble		^{t}RPST	0.33	–	0.33	–	0.33	–			CK	21
Command and Address Timing												
DLL locking time		^{t}DLLK	854	–	940	–	1024	–			CK	2, 4
CMD, ADDR setup time to CK_t, CK_c referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^{t}IS	55	–	48	–	40	–			ps	
	V_{REFCA}	$^{t}IS_{VREF}$	145	–	138	–	130	–			ps	
CMD, ADDR hold time to CK_t, CK_c referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^{t}IH	80	–	73	–	65	–			ps	
	V_{REFCA}	$^{t}IH_{VREF}$	145	–	138	–	130	–			ps	
CTRL, ADDR pulse width for each input		^{t}IPW	385	–	365	–	340	–			ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD								ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP								ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS								ns	12
ACTIVATE-to-ACTIVATE or REF command period		^{t}RC	See Speed Bin Tables for ^{t}RC								ns	12

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size	$^{t}RRD\_S$ (1/2KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.7ns		MIN = greater of 4CK or 2.5ns				CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size	$^{t}RRD\_S$ (1KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.7ns		MIN = greater of 4CK or 2.5ns				CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size	$^{t}RRD\_S$ (2KB)	MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns				CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size	$^{t}RRD\_L$ (1/2KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns				CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size	$^{t}RRD\_L$ (1KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns				CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size	$^{t}RRD\_L$ (2KB)	MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns				CK	1
Four ACTIVATE windows for 1/2KB page size	^{t}FAW (1/2KB)	MIN = greater of 16CK or 12ns		MIN = greater of 16CK or 10.875ns		MIN = greater of 16CK or 10ns				ns	
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns				ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns				ns	
WRITE recovery time	$^{t}WR_{1ck}$	MIN = 15ns								ns	1, 5, 9
	$^{t}WR_{2ck}$	MIN = 1CK + $^{t}WR_{1ck}$								CK	1, 5, 10
WRITE recovery time when CRC and DM are both enabled	$^{t}WR\_CRC\_DM_{1ck}$	MIN = $^{t}WR_{1ck}$ + greater of (5CK or 3.75ns)								CK	1, 6, 9
WRITE recovery time when CRC and DM are both enabled	$^{t}WR\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WR\_CRC\_DM_{1ck}$								CK	1, 6, 10
Delay from start of internal WRITE transaction to internal READ command – Same bank group	$^{t}WTR\_L_{1ck}$	MIN = greater of 4CK or 7.5ns								CK	1, 5, 9
	$^{t}WTR\_L_{2ck}$	MIN = 1CK + $^{t}WTR\_L_{1ck}$								CK	1, 5, 10

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Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	$^{t}WTR\_L\_CRC\_DM_{1ck}$	MIN = $^{t}WTR\_L_{1ck}$ + greater of (5CK or 3.75ns)								CK	1, 6, 9
	$^{t}WTR\_L\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WTR\_L\_CRC\_DM_{1ck}$								CK	1, 6, 10
Delay from start of internal WRITE transaction to internal READ command – Different bank group	$^{t}WTR\_S_{1ck}$	MIN = greater of (2CK or 2.5ns)								CK	1, 5, 7, 8, 9
	$^{t}WTR\_S_{2ck}$	MIN = 1CK + $^{t}WTR\_S_{1ck}$								CK	1, 5, 7, 8, 10
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	$^{t}WTR\_S\_CRC\_DM_{1ck}$	MIN = $^{t}WTR\_S_{1ck}$ + greater of (5CK or 3.75ns)								CK	1, 6, 7, 8, 9
	$^{t}WTR\_S\_CRC\_DM_{2ck}$	MIN = 1CK + $^{t}WTR\_S\_CRC\_DM_{1ck}$								CK	1, 6, 7, 8, 10
READ-to-PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns								CK	1
CAS_n-to-CAS_n command delay to different bank group	$^{t}CCD\_S$	4	–	4	–	4	–			CK	
CAS_n-to-CAS_n command delay to same bank group	$^{t}CCD\_L$	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–			CK	14
Auto precharge write recovery + precharge time	^{t}DAL (MIN)	MIN = WR + ROUND$^{t}RP/^{t}CK$ (AVG); MAX = N/A								CK	8
MRS Command Timing											
MRS command cycle time	^{t}MRD	8	–	8	–	8	–			CK	
MRS command cycle time in PDA mode	$^{t}MRD\_PDA$	MIN = greater of (16nCK, 10ns)									1
MRS command cycle time in CAL mode	$^{t}MRD\_CAL$	MIN = ^{t}MOD + ^{t}CAL								CK	
MRS command update delay	^{t}MOD	MIN = greater of (24nCK, 15ns)								CK	1
MRS command update delay in PDA mode	$^{t}MOD\_PDA$	MIN = ^{t}MOD								CK	
MRS command update delay in CAL mode	$^{t}MOD\_CAL$	MIN = ^{t}MOD + ^{t}CAL								CK	
MRS command to DQS drive in preamble training	^{t}SDO	MIN = ^{t}MOD + 9ns									

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
MPR Command Timing											
Multipurpose register recovery time	^{t}MPRR	MIN = 1nCK								CK	
Multipurpose register write recovery time	^{t}WR_MPR	MIN = ^{t}MOD + AL + PL									
CRC Error Reporting Timing											
CRC error to ALERT_n latency	^{t}CRC_ALERT	3	13	3	13	3	13			ns	
CRC ALERT_n pulse width	^{t}CRC_ALERT_PW	6	10	6	10	6	10			CK	
CA Parity Timing											
Parity latency	PL	5	–	6	–	6	–			CK	
Commands uncertain to be executed during this time	^{t}PAR_UNKNOWN	–	PL	–	PL	–	PL			CK	
Delay from errant command to ALERT_n assertion	^{t}PAR_ALERT_ON	–	PL + 6ns	–	PL + 6ns	–	PL + 6ns			CK	
Pulse width of ALERT_n signal when asserted	^{t}PAR_ALERT_PW	80	160	88	176	96	192			CK	
Time from alert asserted until DES commands required in persistent CA parity mode	^{t}PAR_ALERT_RSP	–	71	–	78	–	85			CK	
CAL Timing											
CS_n to command address latency	^{t}CAL	5	–	6	–	6	–			CK	19
CS_n to command address latency in gear-down mode	^{t}CALg	6	–	8	–	8	–			CK	
MPSM Timing											
Command path disable delay upopn MPSM entry	^{t}MPED	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)								CK	1
Valid clock requirement after MPSM entry	^{t}CKMPE	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)								CK	1
Valid clock requirement before MPSM exit	^{t}CKMPX	MIN = ^{t}CKSRX (MIN)								CK	1
Exit MPSM to commands not requiring a locked DLL	^{t}XMP	^{t}XS (MIN)								CK	
Exit MPSM to commands requiring a locked DLL	^{t}XMPDLL	MIN = ^{t}XMP (MIN) + ^{t}XSDLL (MIN)								CK	1

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
CS setup time to CKE		^{t}MPX_S	MIN = ^{t}IS (MIN) + ^{t}IH (MIN)								ns	
CS_n HIGH hold time to CKE rising edge		^{t}MPX_HH	MIN = ^{t}XP								ns	
CS_n LOW hold time to CKE rising edge		^{t}MPX_LH	12	^{t}XMP-10ns	12	^{t}XMP-10ns	12	^{t}XMP-10ns			ns	
Connectivity Test Timing												
TEN pin HIGH to CS_n LOW – Enter CT mode		^{t}CT_Enable	200	–	200	–	200	–			ns	
CS_n LOW and valid input to valid output		^{t}CT_Valid	–	200	–	200	–	200			ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		^{t}CTCKE_Valid	10	–	10	–	10	–			ns	
Calibration and V_{REFDQ} Train Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	1024	–	1024	–	1024	–			CK	
	Normal operation	^{t}ZQoper	512	–	512	–	512	–			CK	
ZQCS command: Short calibration time		^{t}ZQCS	128	–	128	–	128	–			CK	
The V_{REF} increment/decrement step time		V_{REF_time}	MIN = 150ns									
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		^{t}VREFDQE	MIN = 150ns								ns	1
Exit V_{REFDQ} training mode to the first WRITE command delay		^{t}VREFDQX	MIN = 150ns								ns	1
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = ^{t}RFC1 + 10ns								ns	1
RESET_L pulse low after power stable		^{t}PW_RESET_S	1.0	–	1.0	–	1.0	–			µs	
RESET_L pulse low at power-up		^{t}PW_RESET_L	200	–	200	–	200	–			µs	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200								ms	
RESET_n LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 0								ns	

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Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	^{t}RFC1	MIN = 260								ns	1, 11
		^{t}RFC2	MIN = 160								ns	1, 11
		^{t}RFC4	MIN = 110								ns	1, 11
	8Gb	^{t}RFC1	MIN = 350								ns	1, 11
		^{t}RFC2	MIN = 260								ns	1, 11
		^{t}RFC4	MIN = 160								ns	1, 11
	16Gb	^{t}RFC1	MIN = 350								ns	1, 11
		^{t}RFC2	MIN = 260								ns	1, 11
		^{t}RFC4	MIN = 160								ns	1, 11
Average periodic refresh interval	-40°C ≤ T_C ≤ 85°C	^{t}REFI	MIN = N/A; MAX = 7.8								µs	11
	85°C < T_C ≤ 95°C	^{t}REFI	MIN = N/A; MAX = 3.9								µs	11
	95°C < T_C ≤ 105°C	^{t}REFI	MIN = N/A; MAX = 1.95								µs	11
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = ^{t}RFC1 + 10ns								ns	1
Exit self refresh to commands not requiring a locked DLL in self refresh abort		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)		^{t}XS_FAST	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN)								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + 1*n*CK								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled		^{t}CKESR_par	MIN = ^{t}CKE (MIN) + 1*n*CK + PL								CK	1

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Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)	^{t}CKSRE	MIN = greater of (5CK, 10ns)								CK	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled	^{t}CKSRE_par	MIN = greater of (5CK, 10ns) + PL								CK	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	^{t}CKSRX	MIN = greater of (5CK, 10ns)								CK	1
Power-Down Timing											
Exit power-down with DLL on to any valid command	^{t}XP	MIN = greater of 4CK or 6ns								CK	1
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled.	^{t}XP _PAR	MIN = (greater of 4CK or 6ns) + PL								CK	1
CKE MIN pulse width	^{t}CKE (MIN)	MIN = greater of 3CK or 5ns								CK	1
Command pass disable delay	^{t}CPDED	4	–	4	–	4	–			CK	
Power-down entry to power-down exit timing	^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI								CK	
Begin power-down period prior to CKE registered HIGH	^{t}ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	^{t}ANPD + ^{t}XSDLL								CK	
Power-Down Entry Minimum Timing											
ACTIVATE command to power-down entry	^{t}ACTPDEN	2	–	2	–	2	–			CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	^{t}PRPDEN	2	–	2	–	2	–			CK	
REFRESH command to power-down entry	^{t}REFPDEN	2	–	2	–	2	–			CK	
MRS command to power-down entry	^{t}MRSPDEN	MIN = ^{t}MOD (MIN)								CK	1
READ/READ with auto precharge command to power-down entry	^{t}RDPDEN	MIN = RL + 4 + 1								CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)								CK	1

Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
WRITE command to power-down entry (BC4MRS)	^{t}WRPBC4DEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG)								CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	^{t}WRAPDEN	MIN = WL + 4 + WR + 1								CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	^{t}WRAPBC4DEN	MIN = WL + 2 + WR + 1								CK	1
ODT Timing											
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2								CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2								CK	
R_{TT} dynamic change skew	^{t}ADC	0.28	0.72	0.26	0.74	0.26	0.74			CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	^{t}AONAS	1	9	1	9	1	9			ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	^{t}AOFAS	1	9	1	9	1	9			ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1^{t}CK	6	–	6	–	6	–			CK	
	ODTH8 2^{t}CK	7	–	7	–	7	–				
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1^{t}CK	4	–	4	–	4	–			CK	
	ODTH4 2^{t}CK	5	–	5	–	5	–				
Write Leveling Timing											
First DQS_t, DQS_c rising edge after write leveling mode is programmed	^{t}WLMRD	40	–	40	–	40	–			CK	
DQS_t, DQS_c delay after write leveling mode is programmed	^{t}WLDQSEN	25	–	25	–	25	–			CK	
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	^{t}WLS	0.13	–	0.13	–	0.13	–			CK	
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	^{t}WLH	0.13	–	0.13	–	0.13	–			CK	
Write leveling output delay	^{t}WLO	0	9.5	0	9.5	0	9.5			ns	
Write leveling output error	^{t}WLOE	0	2	0	2	0	2			ns	
Gear-Down Timing											

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Table 167: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Reserved		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Exit reset from CKE HIGH to a valid MRS gear-down	^{t}XPR_GEAR	^{t}XPR		^{t}XPR		^{t}XPR				CK	
CKE HIGH assert to gear-down enable time)	^{t}XS_GEAR	^{t}XS		^{t}XS		^{t}XS				CK	
MRS command to sync pulse time	^{t}SYNC_GEAR	^{t}MOD + 4CK		^{t}MOD + 4CK		^{t}MOD + 4CK				CK	
Sync pulse to first valid command	^{t}CMD_GEAR	^{t}MOD		^{t}MOD		^{t}MOD				CK	
Gear-down setup time	^{t}GEAR_setup	2CK	–	2CK	–	2CK	–			CK	
Gear-down hold time	^{t}GEAR_hold	2CK	–	2CK	–	2CK	–			CK	

Notes:
1. Maximum limit not applicable.
2. Micron tDLLK values support the legacy JEDEC tDLLK specifications.
3. DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.
4. Data rate is greater than or equal to 1066 Mb/s.
5. WRITE-to-READ when CRC and DM are both not enabled.
6. WRITE-to-READ delay when CRC and DM are both enabled.
7. The start of internal write transactions is defined as follows:
   - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
8. For these parameters, the device supports ^{t}nPARAM [nCK] = ROUND{^{t}PARAM [ns]/^{t}CK (AVG) [ns]} according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.
9. When operating in 1^{t}CK WRITE preamble mode.
10. When operating in 2^{t}CK WRITE preamble mode.
11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to ^{t}RFC refresh time.
12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
13. Applicable from ^{t}CK (AVG) MIN to ^{t}CK (AVG) MAX as stated in the Speed Bin tables.
14. JEDEC specifies a minimum of five clocks.
15. The maximum read postamble is bound by ^{t}DQSCK (MIN) plus ^{t}QSH (MIN) on the left side and ^{t}HZ(DQS) MAX on the right side.
16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately 0.7 × V_{DDQ} as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to V_{TT} = V_{DDQ}.
17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.

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18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of ^{t}CK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN.
19. The actual ^{t}CAL minimum is the larger of 3 clocks or 3.748ns/^{t}CK; the table lists the applicable clocks required at targeted speed bin.
20. The maximum READ preamble is bounded by ^{t}LZ(DQS) MIN on the left side and ^{t}DQSCK (MAX) on the right side. See figure in the Clock to Data Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2^{t}CK toggle mode, as illustrated in the READ Preamble section.
21. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
22. The ^{t}PDA_S/^{t}PDA_H parameters may use the ^{t}DS/^{t}DH limits, respectively, if the signal is LOW the entire BL8.

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the MIN/MAX values may result in malfunction of the DDR4 SDRAM device.

Definition for ^{t}CK(AVG)

^{t}CK(AVG) is calculated as the average clock period across any consecutive 200-cycle window, where each clock period is calculated from rising edge to rising edge.

$$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CK_j\right) / N$$

Where N = 200

Definition for ^{t}CK(ABS)

^{t}CK(ABS) is defined as the absolute clock period as measured from one rising edge to the next consecutive rising edge. ^{t}CK(ABS) is not subject to a production test.

Definition for ^{t}CH(AVG) and ^{t}CL(AVG)

^{t}CH(AVG) is defined as the average high pulse width as calculated across any consecutive 200 high pulses.

$$^{t}CH(AVG) = \left(\sum_{j=1}^{N} {}^{t}CH_j\right) / (N \times {}^{t}CK(AVG))$$

Where N = 200

^{t}CL(AVG) is defined as the average low pulse width as calculated across any consecutive 200 low pulses.

$$^{t}CL(AVG) = \left(\sum_{j=1}^{N} {}^{t}CL_j\right) / (N \times {}^{t}CK(AVG))$$

Where N = 200

Definition for ^{t}JIT(per) and ^{t}JIT(per,lck)

^{t}JIT(per) is defined as the largest deviation of any signal ^{t}CK from ^{t}CK(AVG).

^{t}JIT(per) = MIN/MAX of {^{t}CKi - ^{t}CK(AVG) where i = 1 to 200}.

^{t}JIT(per) defines the single period jitter when the DLL is already locked.

^{t}JIT(per,lck) uses the same definition for single period jitter, but only during the DLL locking period.

^{t}JIT(per) and ^{t}JIT(per,lck) are not subject to production test.

Definition for ^{t}JIT(cc) and ^{t}JIT(cc,lck)

^{t}JIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

^{t}JIT(cc) = MAX of |{^{t}CKi +1 - ^{t}CKi}|.

^{t}JIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

^{t}JIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

^{t}JIT(cc) and ^{t}JIT(cc,lck) are not subject to production test.

Definition for ^{t}ERR(nper)

^{t}ERR is defined as the cumulative error across *n* multiple consecutive cycles from ^{t}CK(AVG). ^{t}ERR is not subject to a production test.

Jitter Notes

Note a: Unit ^{t}CK(AVG) represents the actual ^{t}CK(AVG) of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, including the actual clock edges. Example: ^{t}MRD = 4 [*n*CK] means that if one MODE REGISTER SET command is registered at Tm, another MODE REGISTER SET command may be registered at Tm + 4, even if (Tm + 4 - Tm) is (4 × ^{t}CK(AVG) + ^{t}ERR (4 per) MIN).

Note b: These parameters are measured from a command/address signal (such as CKE, CS_n, RAS_n, CAS_n, WE_n, ODT, BA0, A0, or A1) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the amount of clock jitter applied (for example, ^{t}JITper, ^{t}JITcc) because the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Note c: These parameters are measured from a data strobe signal (DQS_t[L/U], DQS_c[L/U]) crossing to its respective clock signal (CK_t, CK_c) crossing. The specification values are not affected by the amount of clock jitter applied (for example, ^{t}JITper, ^{t}JITcc) because these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Note d: These parameters are measured from a data signal (such as DM[L/U], DQ[L/U]0, or DQ[L/U]1) transition edge to its respective data strobe signal (DQS_t[L/U], DQS_c[L/U]) crossing.

Note e: For these parameters, the DDR4 SDRAM device supports ^{t}*n*PARAM [*n*CK] = RU[^{t}PARAM [ns]/^{t}CK(AVG) [ns]], which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support ^{t}*n*RP = RU [^{t}RP/^{t}CK(AVG)], which is in clock cycles, if all input clock jitter specifications are met. This means that for DDR4-800 6-6-6, ^{t}RP = 15ns, the device will support ^{t}*n*RP = RU[^{t}RP/^{t}CK(AVG)] = 6, as long as the input clock jitter specifications are met. For example, the PRECHARGE command at Tm and ACTIVE command at Tm + 6 is valid even if (Tm + 6 - Tm) is less than 15ns due to input clock jitter.

Note f: When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}ERR(mper), act of the input clock, where 2 ≤ *m* ≤ 12 (output deratings are relative to the SDRAM input clock). For example, if the measured jitter into a DDR4-800 SDRAM has ^{t}ERR(mper), act, MIN = –172ps and ^{t}ERR(mper), act, MAX = +193ps, then ^{t}DQSCK, MIN(derated) = ^{t}DQSCK, MIN - ^{t}ERR(mper), act, MAX = –400ps - 193ps = –593ps and ^{t}DQSCK, MAX(derated) = ^{t}DQSCK, MAX - ^{t}ERR(mper), act, MIN = 400ps + 172ps = 572ps. Similarly, ^{t}LZ(DQ) for DDR4-800 derates to ^{t}LZ(DQ), MIN(derated) = –800ps - 193ps = –993ps and ^{t}LZ(DQ), MAX(derated) = 400ps + 172ps = 572ps. Note that ^{t}ERR(mper), act, MIN is the minimum measured value of ^{t}ERR(nper) where 2 ≤ *n* ≤ 12, and ^{t}ERR(mper), act, MAX is the maximum measured value of ^{t}ERR(nper) where 2 ≤ *n* ≤ 12.

Note g: When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JIT(per), act of the input clock (output deratings are relative to the SDRAM input clock). For example, if the measured jitter into a DDR4-800 SDRAM has ^{t}CK(AVG), act = 2500ps, ^{t}JIT(per), act, MIN

= –72ps and ^{t}JIT(per), act, MAX = +93ps, then ^{t}RPRE, MIN(derated) = ^{t}RPRE, MIN + ^{t}JIT(per), act, MIN = 0.9 × ^{t}CK(AVG), act + ^{t}JIT(per), act, MIN = 0.9 × 2500ps - 72ps = 2178ps. Similarly, ^{t}QH, MIN(derated) = ^{t}QH, MIN + ^{t}JIT(per), act, MIN = 0.38 × ^{t}CK(AVG), act + ^{t}JIT(per), act, MIN = 0.38 × 2500ps - 72ps = 878ps.

Converting Time-Based Specifications to Clock-Based Requirements

Software algorithms for calculation of timing parameters are subject to potential rounding errors when converting DRAM timing requirements to system clocks; for example, a memory clock with a nominal frequency of 933.33...3 MHz which yields a clock period of 1.071428571429...ns. It is unrealistic to represent all digits after the decimal point exactly and some sort of rounding needs to be done.

DDR4 SDRAM SPD-based specifications use a minimum granularity for SPD-associated timing parameters of 1ps. Clock periods such as ^{t}CK (AVG) MIN are defined to the nearest picosecond. For example, 1.071428571429...ns is stated as 1071ps. Parameters such as ^{t}AA MIN are specified in units of time (nanoseconds) and require mathematical computation to convert to system clocks (*n*CK). Rules for rounding allow optimization of device performance without violating device parameters. These SPD algorithms rely on results that are within *n*CK adjustment factors on device testing and specification to avoid losing performance due to rounding errors when using SPD-based parameters. Note that JEDEC also defines an *n*CK adjustment factor, but mandates the inverse *n*CK adjustment factor be used in case of conflicting results, so only the inverse *n*CK adjustment factor is discussed here.

Guidance converting SPD associated timing parameters to system clock requirements:

- Round the application clock period up to the nearest picosecond.
- Express the timing specification and application clock period in picoseconds; scaling a nanosecond-based parameter value by 1000 allows programmers to use integer math instead of real math by expressing timing in ps.
- Divide the picosecond-based parameter by the picoseconds based application clock period.
- Add an inverse *n*CK adjustment factor of 97.4%.
- Truncate down to the next lower integer value.
- *n*CK = Truncate[(parameter in ps)/(application ^{t}CK in ps) + (974/1000)].

Guidance converting nonSPD associated timing parameters to system clock requirements:

- Divide the time base specification (in ns) and divided by the clock period (in ns).
- The resultant is set to the next higher integer number of clocks.
- *n*CK = Ceiling[(parameter in ns/application ^{t}CK in ns)].

Options Tables

Table 168: Options – Speed Based

Function	Acronym	Data Rate						
		1600	1866	2133	2400	2666	2933	3200
Write leveling	WL	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temperature controlled refresh	TCR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Low-power auto self refresh	LPASR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fine granularity refresh	FGR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multipurpose register	MR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Data mask	DM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Data bus inversion	DBI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
TDQS	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ZQ calibration	ZQ CAL	Yes	Yes	Yes	Yes	Yes	Yes	Yes
V_{REFDQ} calibration	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Per-DRAM addressability	Per DRAM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mode register readout	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Command/Address latency	CAL	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Write CRC	CRC	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CA parity	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gear-down mode	–	**No**	**No**	**No**	**No**	Yes	Yes	Yes
Programmable preamble	–	**No**	**No**	**No**	Yes	Yes	Yes	Yes
Maximum power saving mode	MPSM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Additive latency	AL	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Connectivity test mode	CT	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hard post package repair mode	hPPR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Soft post package repair mode	sPPR	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MBIST-PPR	MBIST-PPR	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 169: Options – Width Based

Function	Acronym	Width		
		x4	x8	x16
Write leveling	WL	Yes	Yes	Yes
Temperature controlled refresh	TCR	Yes	Yes	Yes
Low-power auto self refresh	LPASR	Yes	Yes	Yes
Fine granularity refresh	FGR	Yes	Yes	Yes
Multipurpose register	MR	Yes	Yes	Yes
Data mask	DM	**No**	Yes	Yes
Data bus inversion	DBI	**No**	Yes	Yes
TDQS	–	**No**	Yes	**No**
ZQ calibration	ZQ CAL	Yes	Yes	Yes
V_{REFDQ} calibration	–	Yes	Yes	Yes
Per-DRAM addressability	Per DRAM	Yes	Yes	Yes
Mode regsiter readout	–	Yes	Yes	Yes
Command/Address latency	CAL	Yes	Yes	Yes
Write CRC	CRC	Yes	Yes	Yes
CA parity	–	Yes	Yes	Yes
Gear-down mode	–	Yes	Yes	Yes
Programmable preamble	–	Yes	Yes	Yes
Maximum power-down mode	MPSM	Yes	Yes	Yes
Additive latency	AL	Yes	Yes	Yes
Connectivity test mode	CT	JEDEC optional on 8Gb and larger densities **Micron supports on all densities**		Yes
Hard post package repair mode	hPPR	JEDEC optional on 4Gb **Micron supports on all densities**		
Soft post package repair mode	sPPR	JEDEC optional on 4Gb and 8Gb **Micron supports on all densities**		
MBIST-PPR	MBIST-PPR	JEDEC optional **Micron supports only on 8Gb Die Rev R and 16Gb Die Rev F**		

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