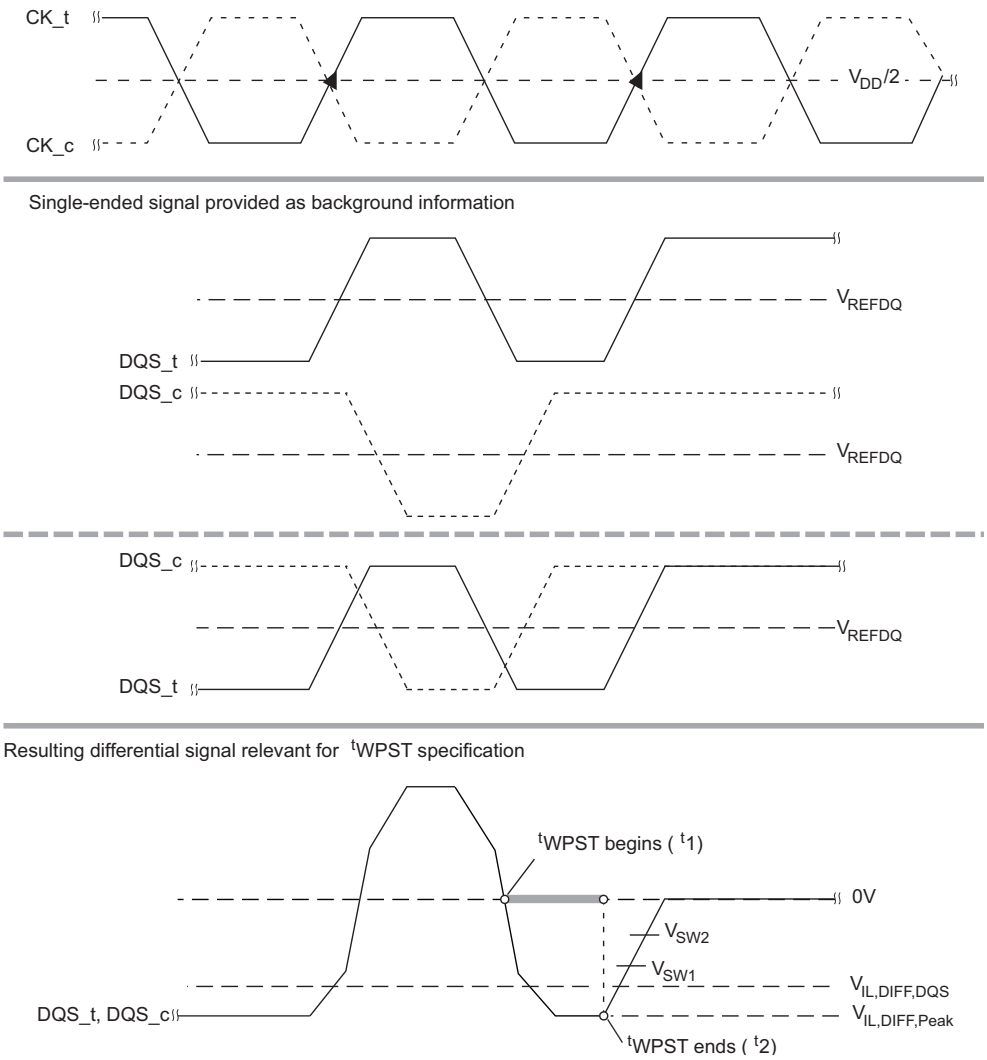
tWPST Calculation

Figure 167: tWPST Method for Calculating Transitions and Endpoints

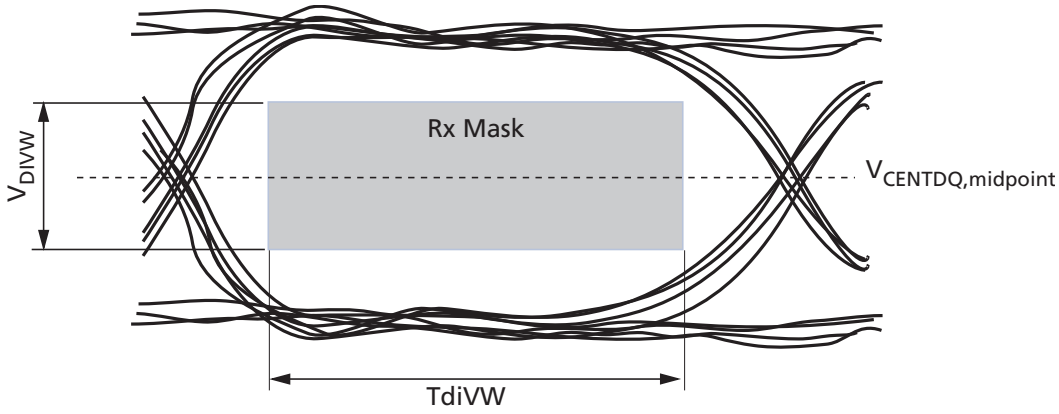


Notes: 1. V_{sw1} =(0.9) × $V_{IL,diff,DQS}$.
2. V_{sw2} = (0.1) × $V_{IL,diff,DQS}$.

Write Timing – Data Strobe-to-Data Relationship

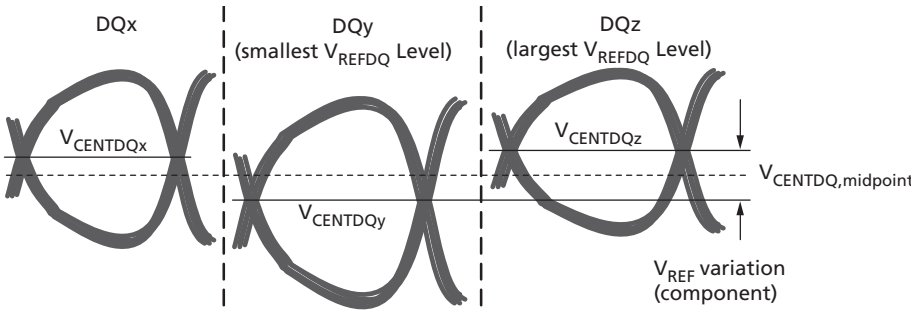
The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx mask) defines the area where the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. The Rx mask is not the valid data-eye. TdiVW and V_{diVW} define the absolute maximum Rx mask.

Figure 168: Rx Compliance Mask



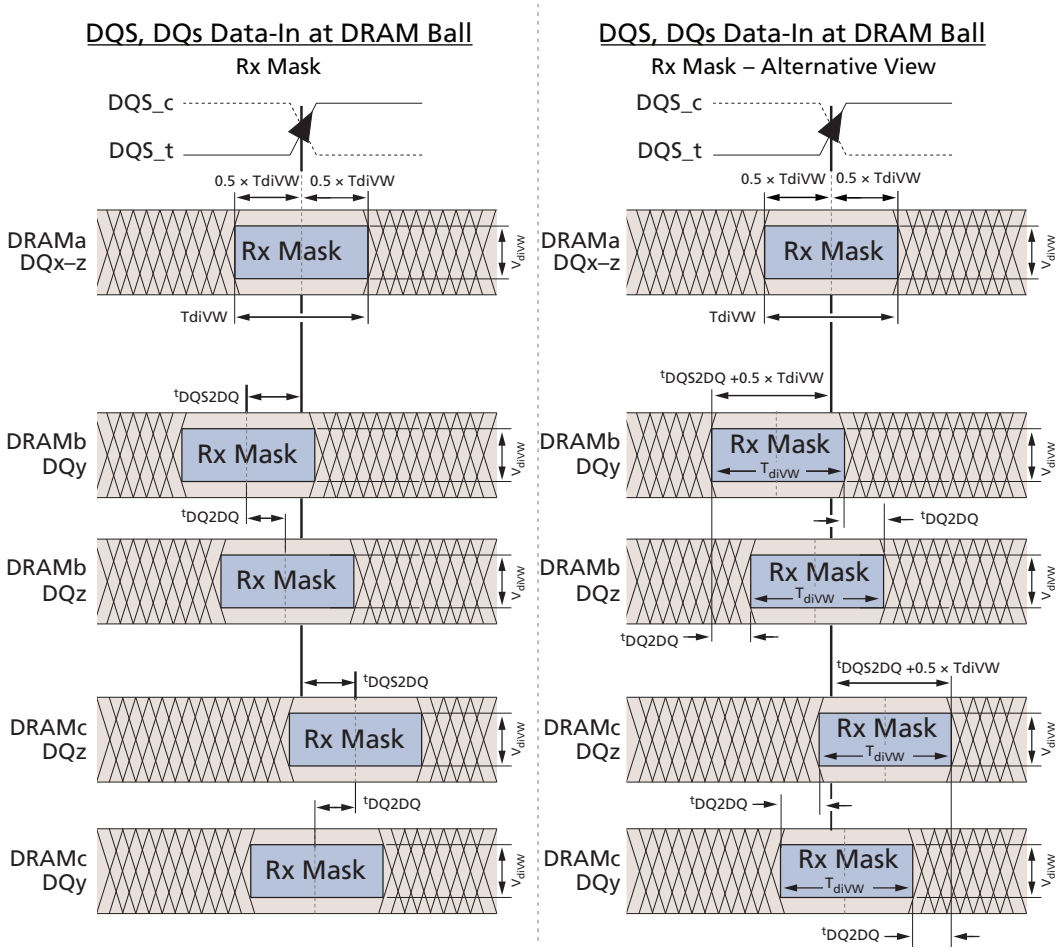
$V_{CENTDQ,midpoint}$ is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM. Each DQ pin's V_{REFDQ} is defined by the center (widest opening) of the cumulative data input eye as depicted in the following figure. This means a DRAM's level variation is accounted for within the DRAM Rx mask. The DRAM V_{REFDQ} level will be set by the system to account for R_{ON} and ODT settings.

Figure 169: V_{CENT_DQ} V_{REFDQ} Voltage Variation



The following figure shows the Rx mask requirements both from a midpoint-to-midpoint reference (left side) and from an edge-to-edge reference. The intent is not to add any new requirement or specification between the two but rather how to convert the relationship between the two methodologies. The minimum data-eye shown in the composite view is not actually obtainable due to the minimum pulse width requirement.

Figure 170: Rx Mask DQ-to-DQS Timings



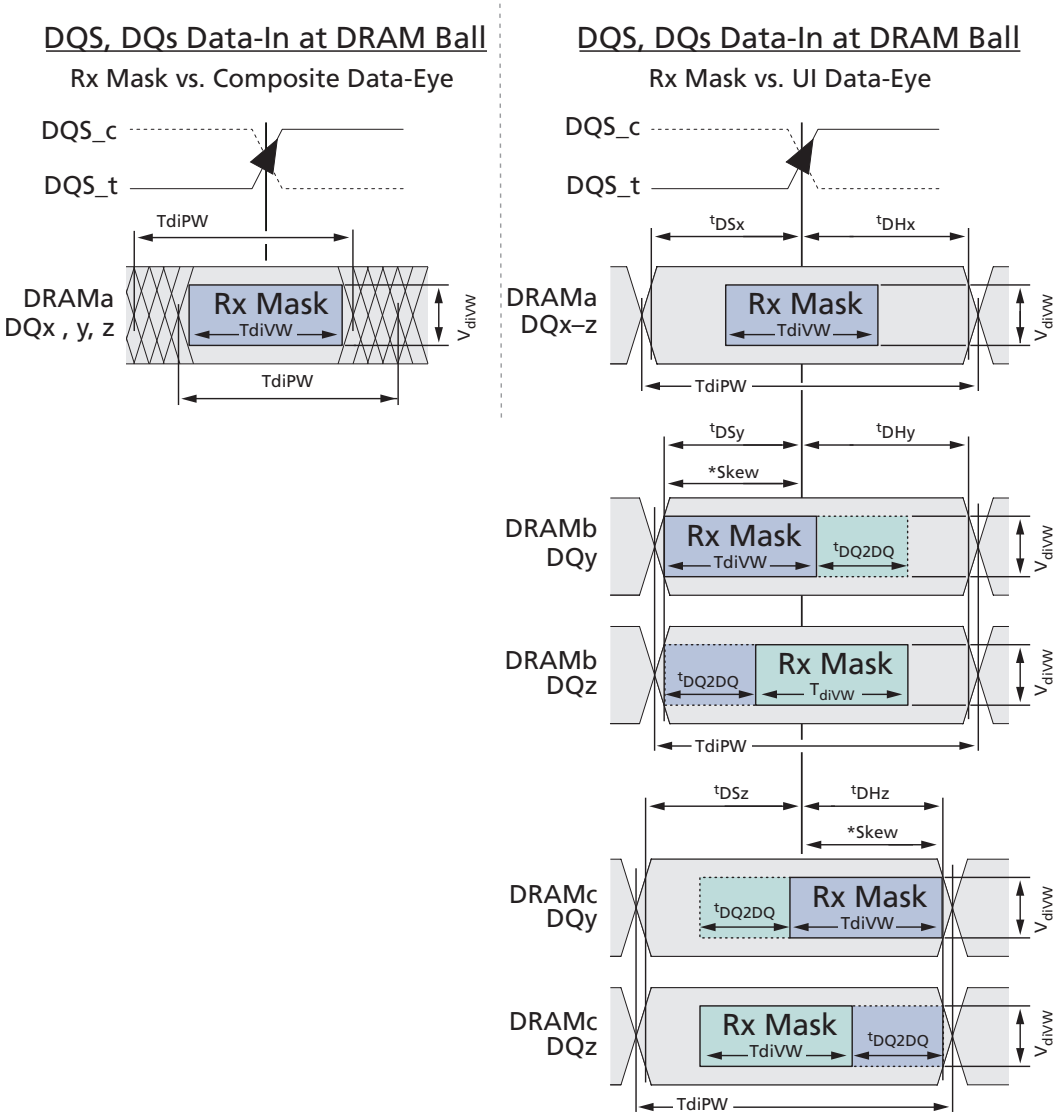
Notes: 1. DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

2. DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with early skews (negative ^{t}DQS2DQ).
DRAMc represents a DRAM with delayed skews (positive ^{t}DQS2DQ).

3. This figure shows the skew allowed between DRAM-to-DRAM and between DQ-to-DQ for a DRAM. Signals assume data is center-aligned at DRAM latch.
TdiPW is not shown; composite data-eyes shown would violate TdiPW.
$V_{CENTDQ,midpoint}$ is not shown but is assumed to be midpoint of V_{diVW}.

The previous figure shows the basic Rx mask requirements. Converting the Rx mask requirements to a classical DQ-to-DQS relationship is shown in the following figure. It should become apparent that DRAM write training is required to take full advantage of the Rx mask.

Figure 171: Rx Mask DQ-to-DQS DRAM-Based Timings



Notes: 1. DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

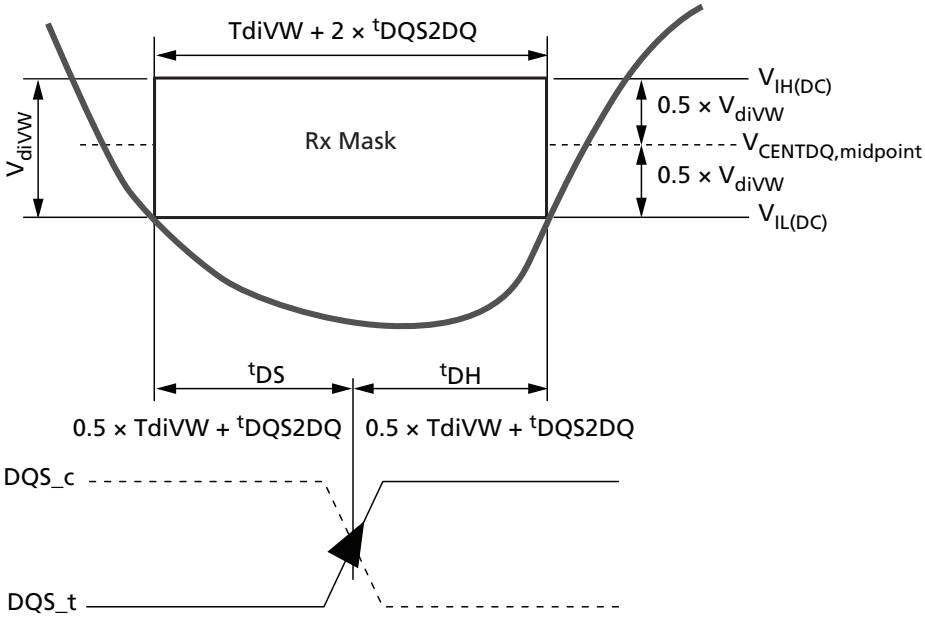
2. *Skew = ^{t}DQS2DQ + 0.5 × TdiVW
DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with the earliest skews (negative ^{t}DQS2DQ, ^{t}DQSy > *Skew).
DRAMc represents a DRAM with the latest skews (positive ^{t}DQS2DQ, ^{t}DQHz > *Skew).

3. ^{t}DS/^{t}DH are traditional data-eye setup/hold edges at DC levels.
^{t}DS and ^{t}DH are not specified; ^{t}DH and ^{t}DS may be any value provided the pulse width and Rx mask limits are not violated.
^{t}DH (MIN) > TdiVW + ^{t}DS (MIN) + ^{t}DQ2DQ.

The DDR4 SDRAM's input receivers are expected to capture the input data with an Rx mask of TdiVW provided the minimum pulse width is satisfied. The DRAM controller will have to train the data input buffer to utilize the Rx mask specifications to this maximum benefit. If the DRAM controller does not

train the data input buffers, then the worst case limits have to be used for the Rx mask (TdiVW + 2 × ^{t}DQS2DQ), which will generally be the classical minimum (^{t}DS and ^{t}DH) and is required as well.

Figure 172: Example of Data Input Requirements Without Training



WRITE Burst Operation

The following write timing diagrams are intended to help understand each write parameter's meaning and are only examples. Each parameter will be defined in detail separately. In these write timing diagrams, CK and DQS are shown aligned, and DQS and DQ are shown center-aligned for the purpose of illustration.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

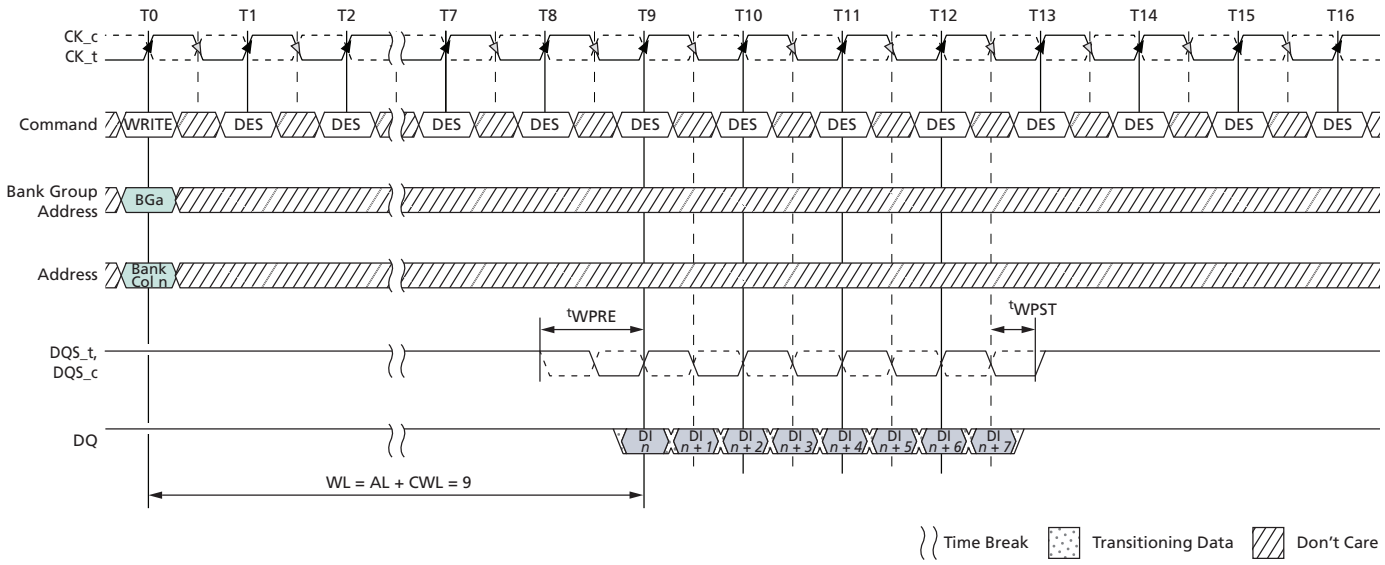
WRITE commands can issue precharge automatically with a WRITE with auto precharge (WRA) command, which is enabled by A10 HIGH.

- WRITE command with A10 = 0 (WR) performs standard write, bank remains active after WRITE burst
- WRITE command with A10 = 1 (WRA) performs write with auto precharge, bank goes into precharge after WRITE burst

The DATA MASK (DM) function is supported for the x8 and x16 configurations only (the DM function is not supported on x4 devices). The DM function shares a common pin with the DBI_n and TDQS functions. The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

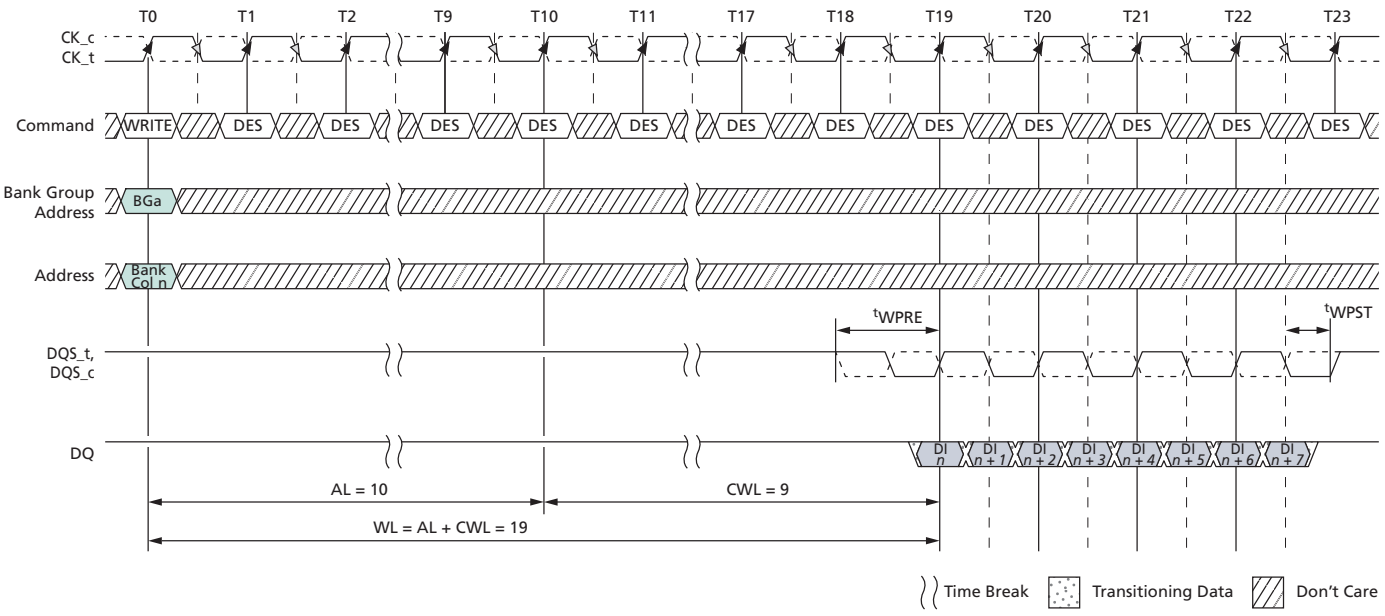
- If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs.
- If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core.
- If CRC write is enabled, then DM enabled (via MRS) will be selected between write CRC nonpersistent mode (DM disabled) and write CRC persistent mode (DM enabled).

Figure 173: WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8)



Notes: 1. BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* = Data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

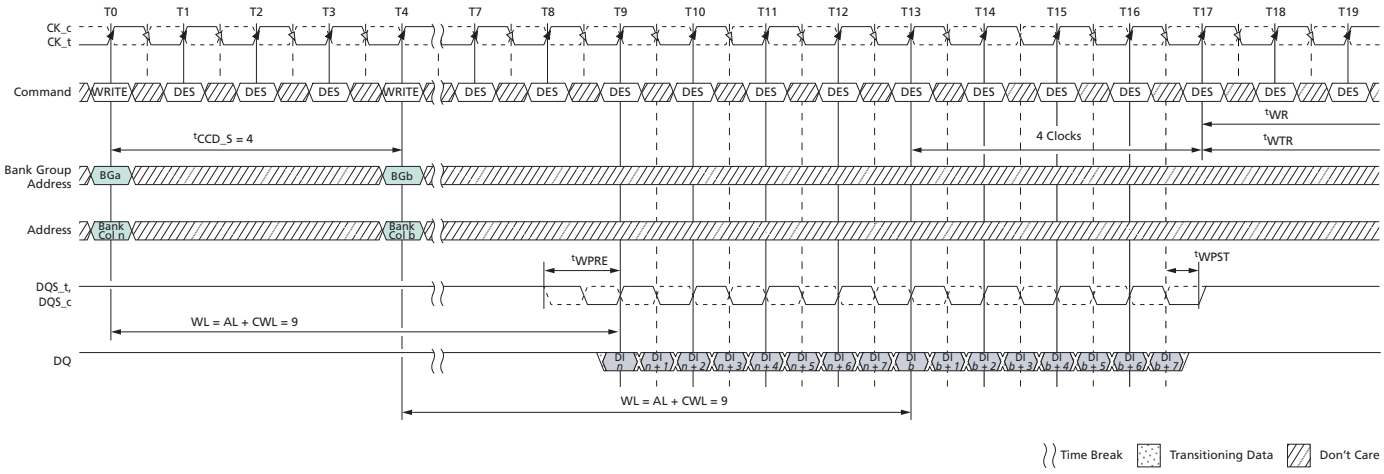
Figure 174: WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)



Notes: 1. BL8, WL = 19, AL = 10 (CL - 1), CWL = 9, Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

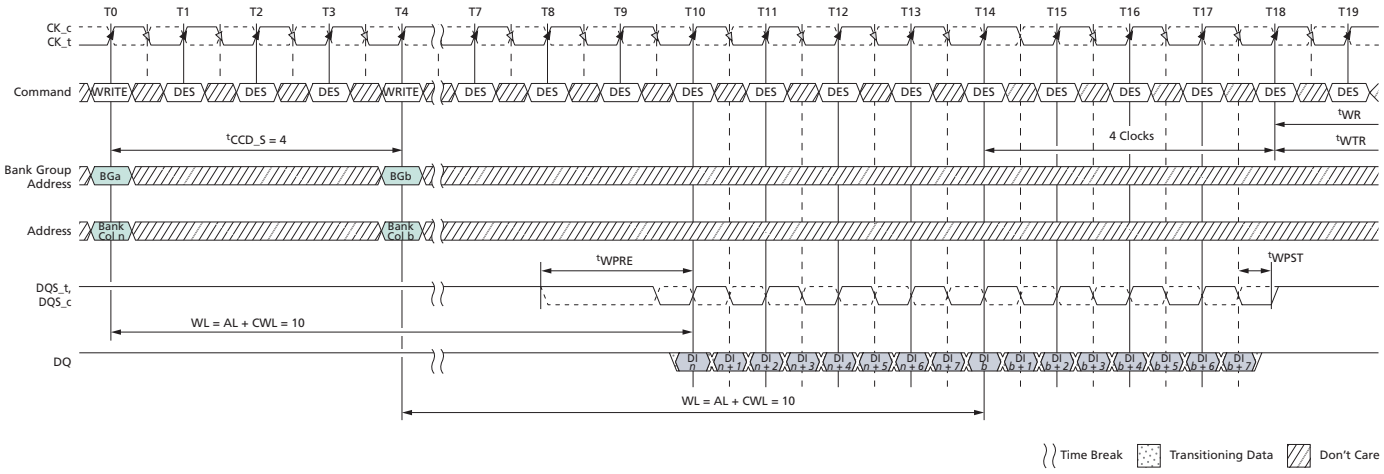
WRITE Operation Followed by Another WRITE Operation

Figure 175: Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



Notes: 1. BL8, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

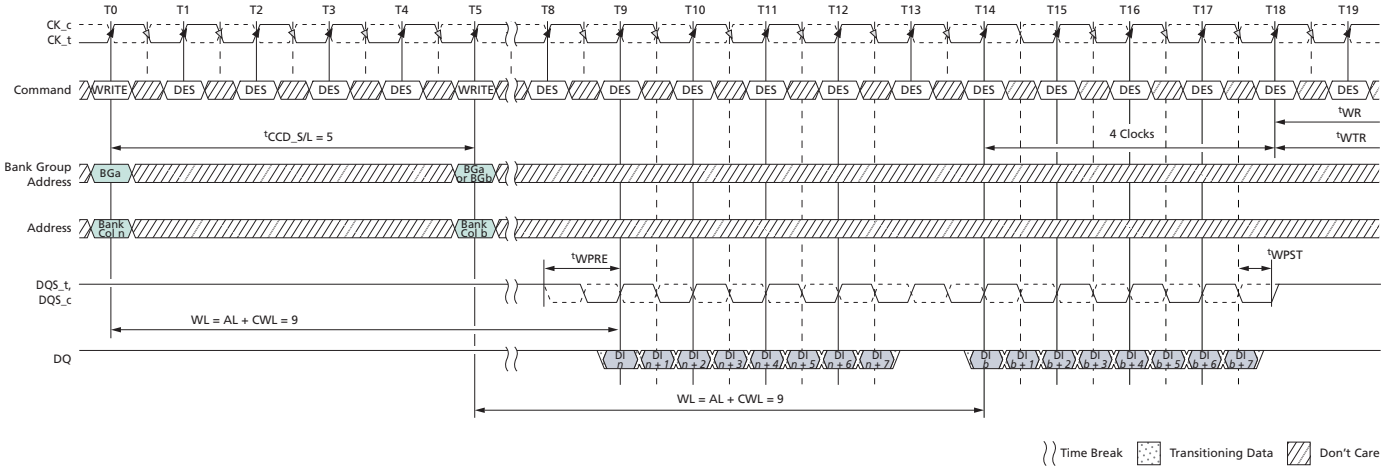
Figure 176: Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



Notes: 1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

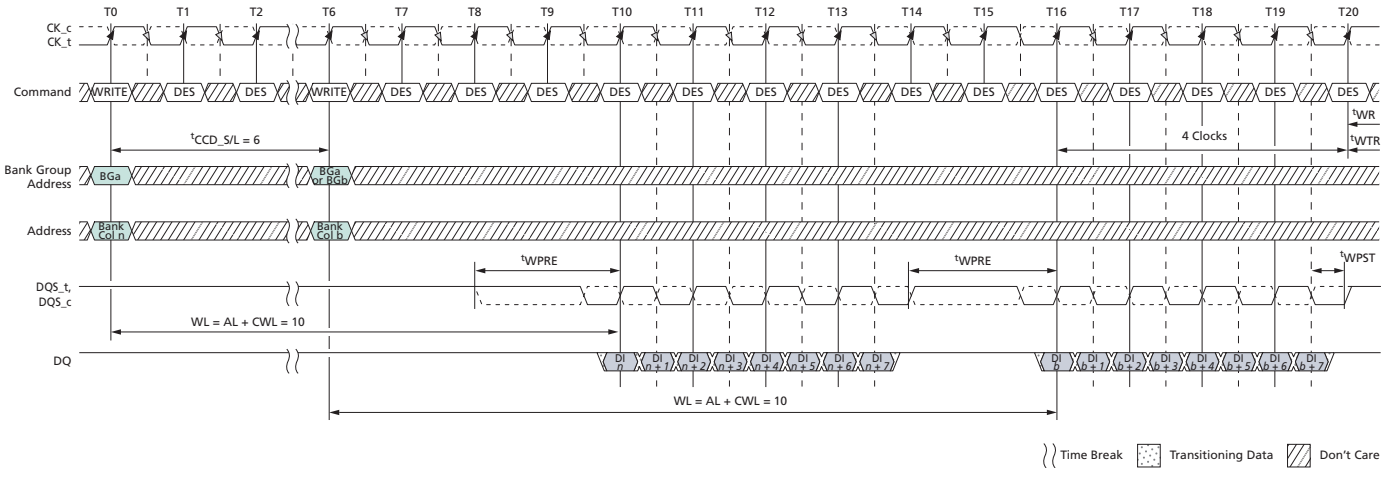
7. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range, which means CWL = 9 is not allowed when operating in 2tCK WRITE preamble mode.

Figure 177: Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



Notes: 1. BL8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

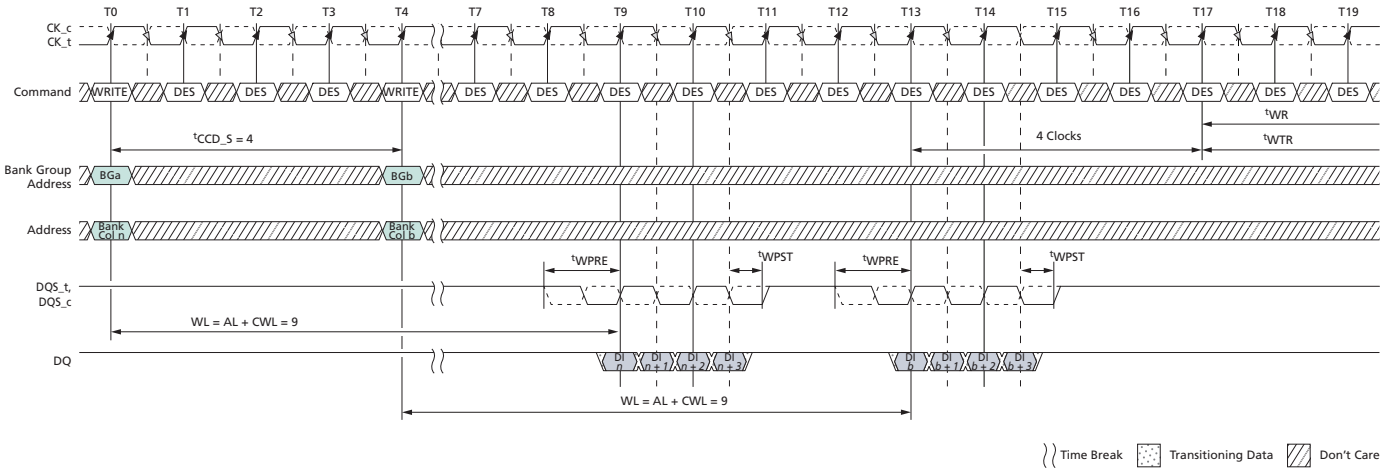
Figure 178: Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



Notes: 1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 8), Preamble = 2tCK, tCCD_S/L = 6tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

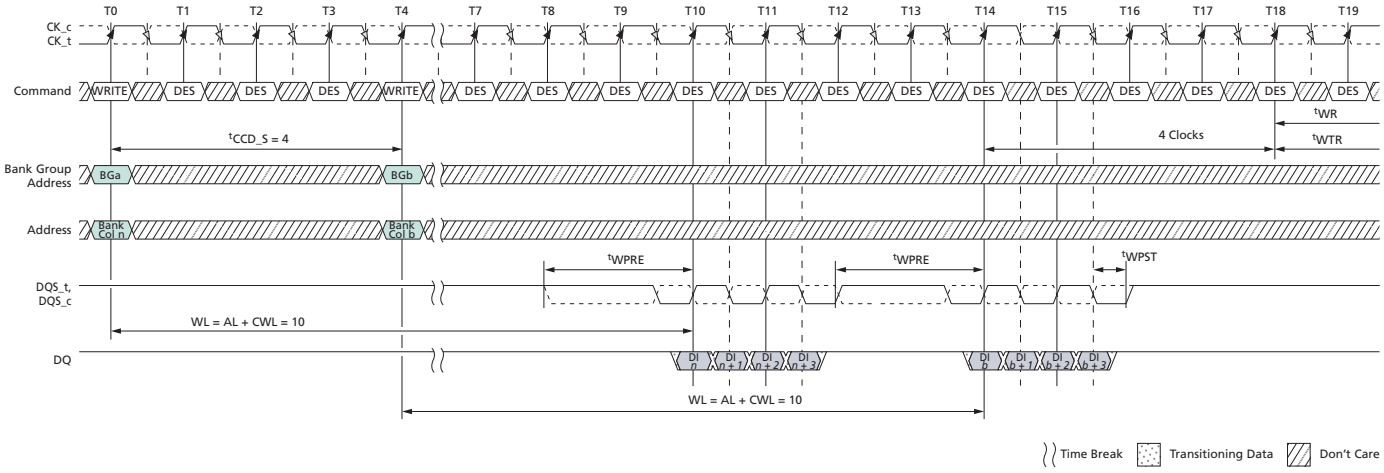
7. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2^{t}CK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range, which means CWL = 9 is not allowed when operating in 2^{t}CK WRITE preamble mode.

Figure 179: WRITE (BC4) OTF to WRITE (BC4) OTF with 1^{t}CK Preamble in Different Bank Group



Notes: 1. BC4, AL = 0, CWL = 9, Preamble = 1^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.

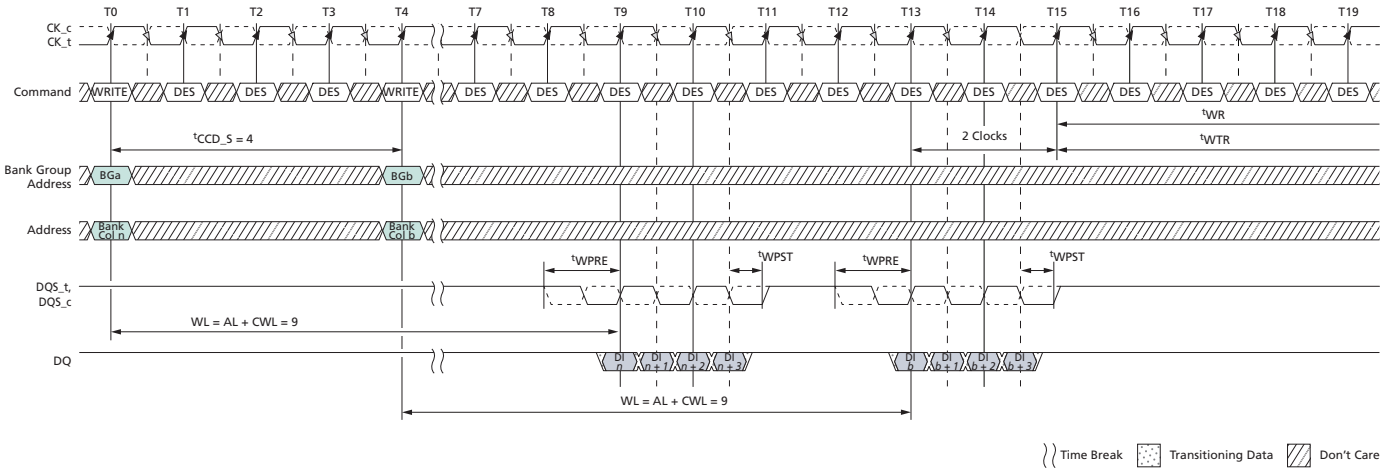
Figure 180: WRITE (BC4) OTF to WRITE (BC4) OTF with 2^{t}CK Preamble in Different Bank Group



Notes: 1. BC4, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.

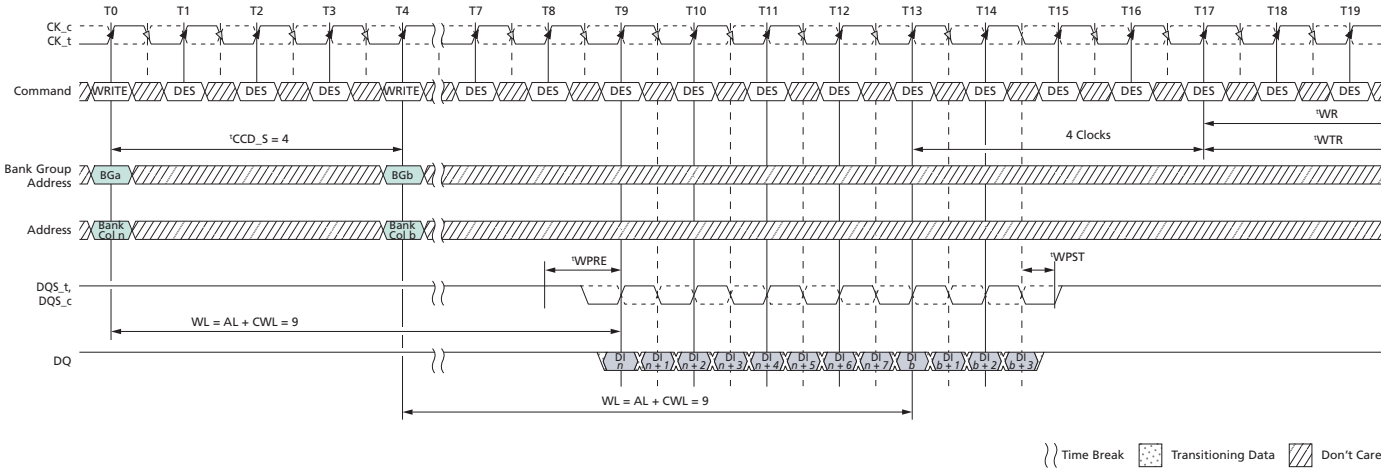
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2^{t}CK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range, which means CWL = 9 is not allowed when operating in 2^{t}CK WRITE preamble mode.

Figure 181: WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1^{t}CK Preamble in Different Bank Group



Notes: 1. BC4, AL = 0, CWL = 9, Preamble = 1^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T15.

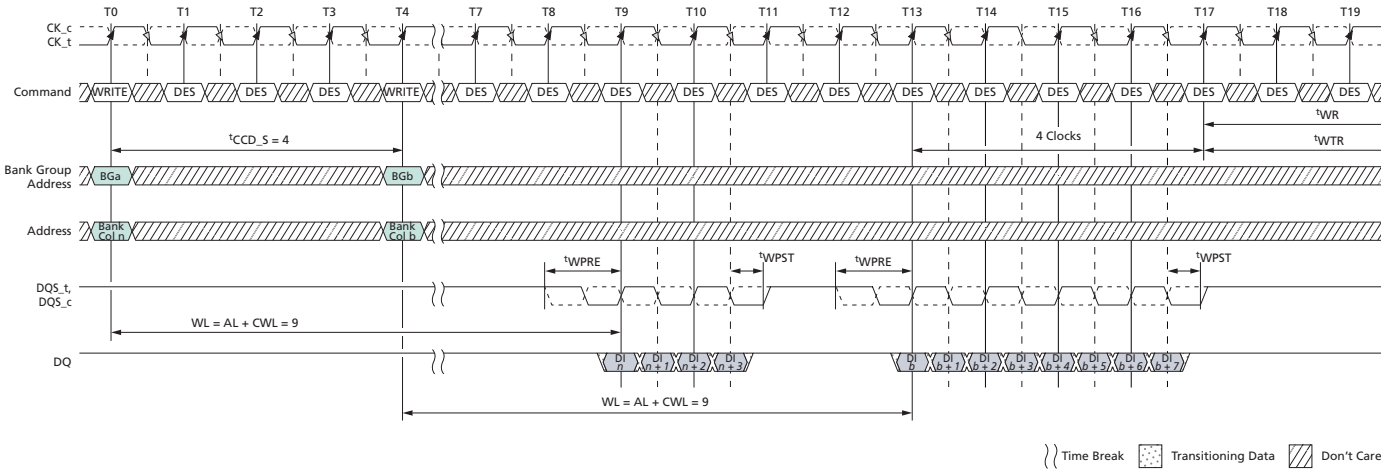
Figure 182: WRITE (BL8) to WRITE (BC4) OTF with 1^{t}CK Preamble in Different Bank Group



Notes: 1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = 1^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T4.

5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.

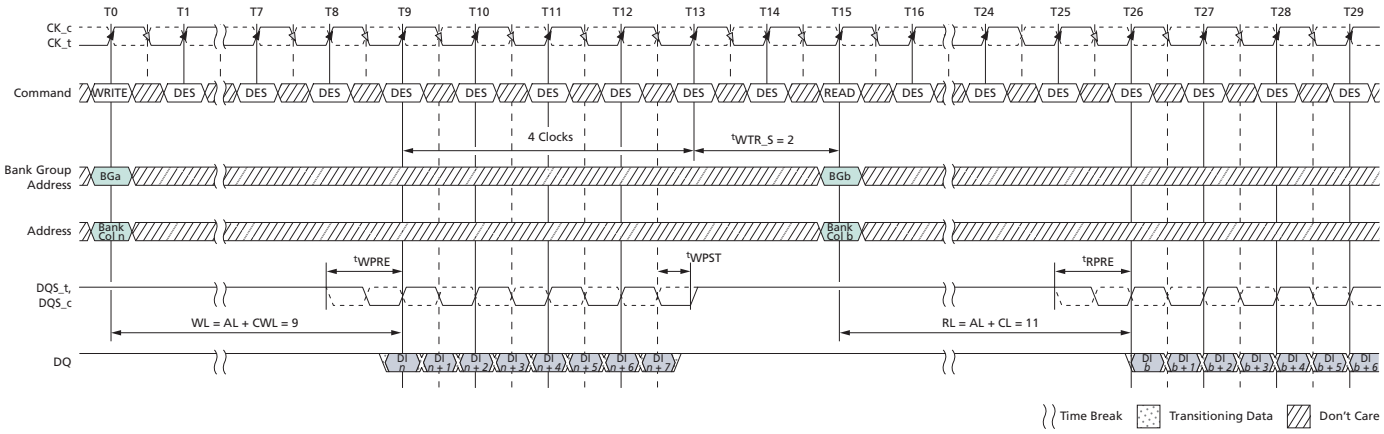
Figure 183: WRITE (BC4) OTF to WRITE (BL8) with 1^{t}CK Preamble in Different Bank Group



Notes: 1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = 1^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
   BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE Operation Followed by READ Operation

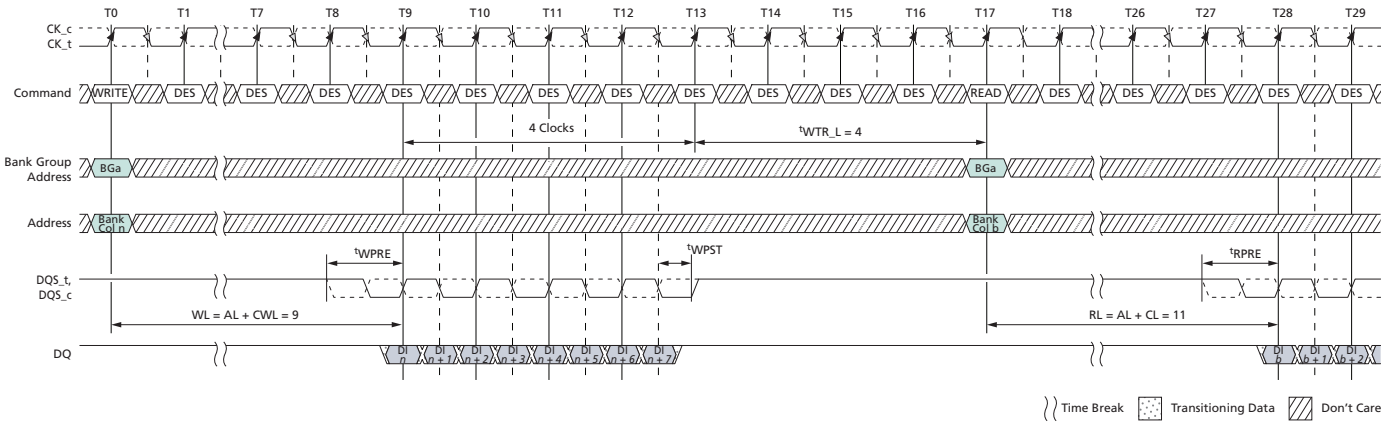
Figure 184: WRITE (BL8) to READ (BL8) with 1^{t}CK Preamble in Different Bank Group



Notes: 1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t}CK, WRITE preamble = 1^{t}CK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T15.

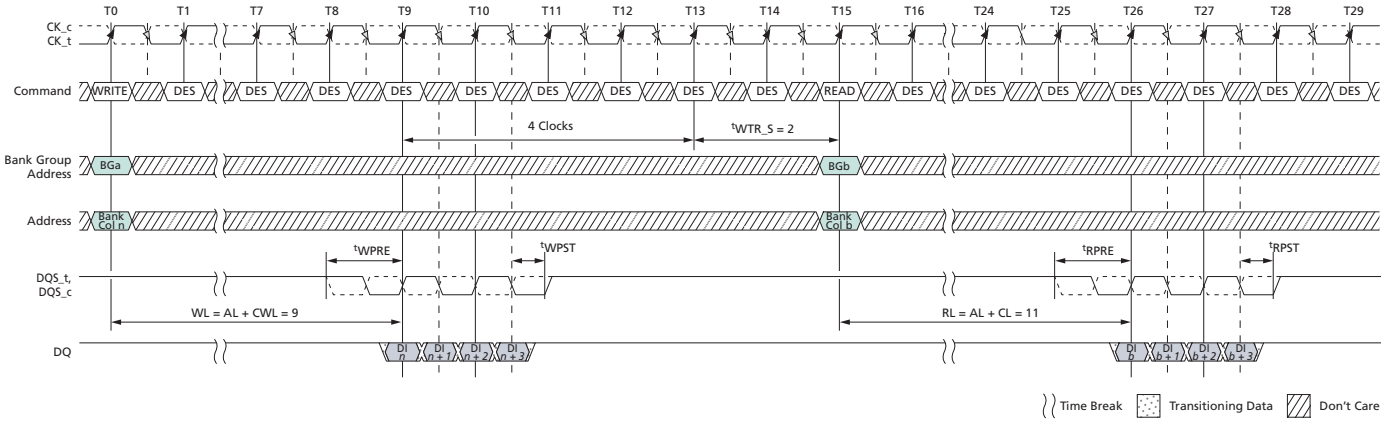
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (^{t}WTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 185: WRITE (BL8) to READ (BL8) with 1^{t}CK Preamble in Same Bank Group



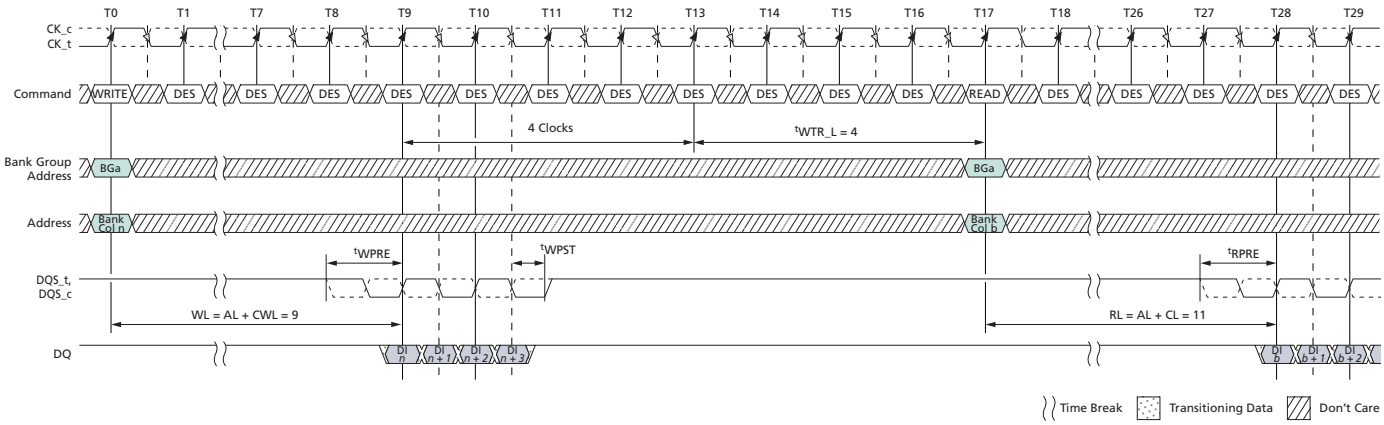
Notes: 1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t}CK, WRITE preamble = 1^{t}CK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (^{t}WTR_L) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 186: WRITE (BC4) OTF to READ (BC4) OTF with 1^{t}CK Preamble in Different Bank Group



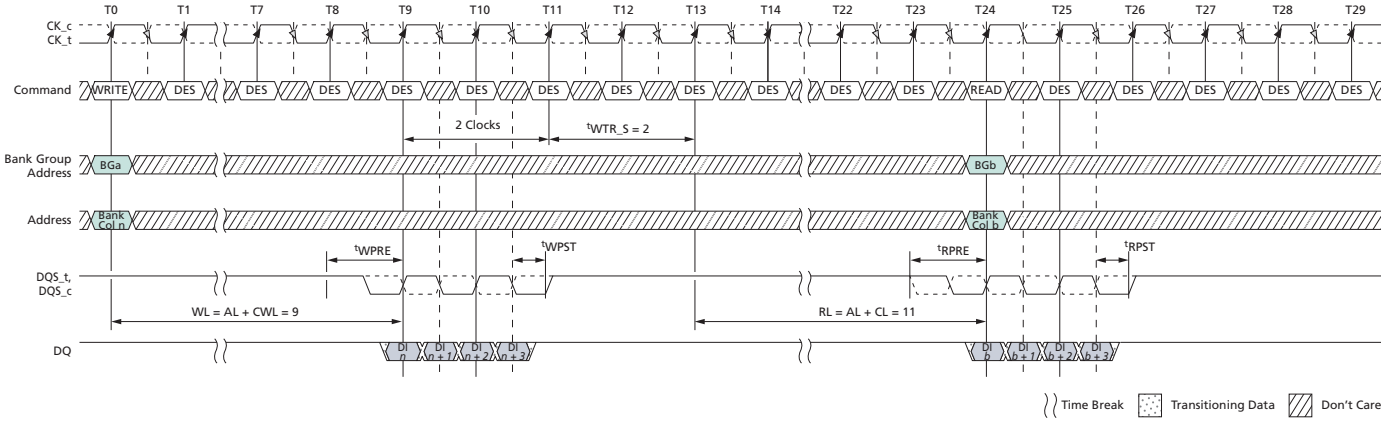
Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^{t}CK, WRITE preamble = 1^{t}CK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (^{t}WTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 187: WRITE (BC4) OTF to READ (BC4) OTF with 1tCK Preamble in Same Bank Group



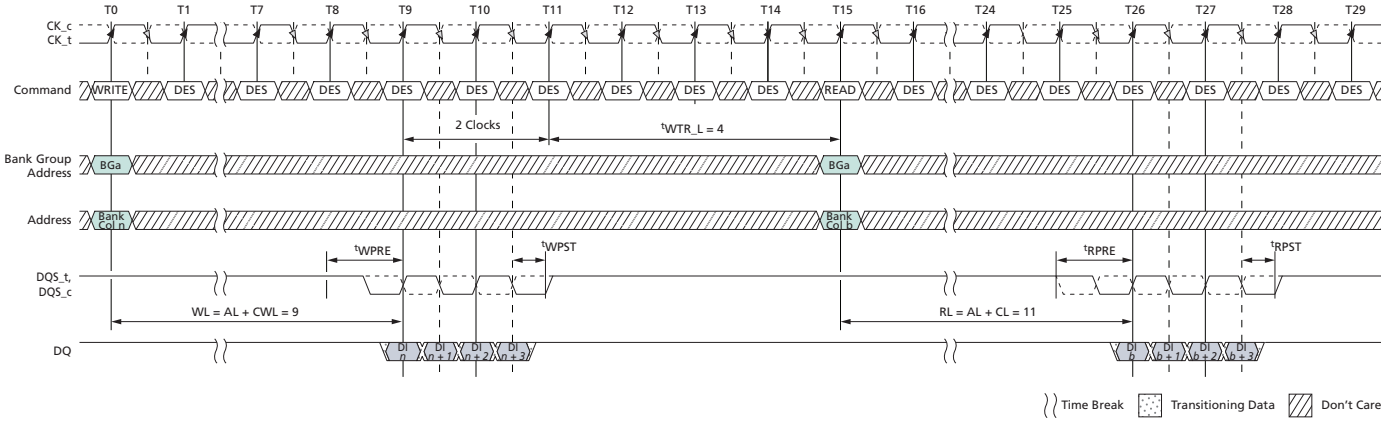
Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T17.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_L) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 188: WRITE (BC4) Fixed to READ (BC4) Fixed with 1 tCK Preamble in Different Bank Group



Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1 tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_S) is referenced from the first rising clock edge after the last write data shown at T11.

Figure 189: WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group

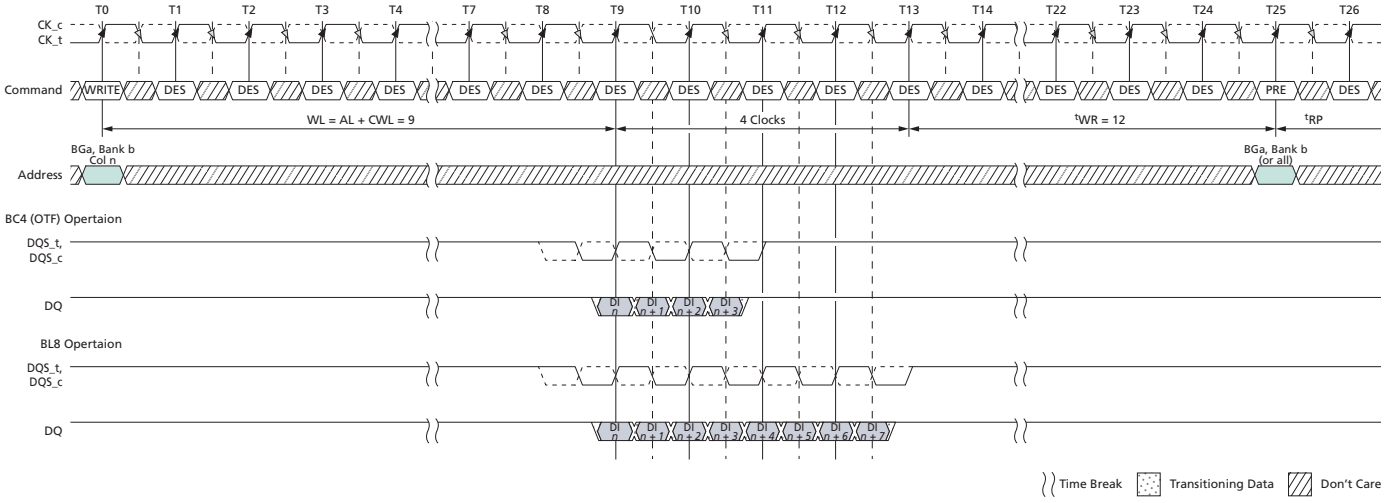


Notes: 1. BC = 4, WL = 9 (CWL = 9, AL = 0), C L = 11, READ preamble = 1tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_L) is referenced from the first rising clock edge after the last write data shown at T11.

WRITE Operation Followed by PRECHARGE Operation

The minimum external WRITE command to PRECHARGE command spacing is equal to WL (AL + CWL) plus either 4tCK (BL8/BC4-OTF) or 2tCK (BC4-fixed) plus tWR. The minimum ACT to PRE timing, tRAS, must be satisfied as well.

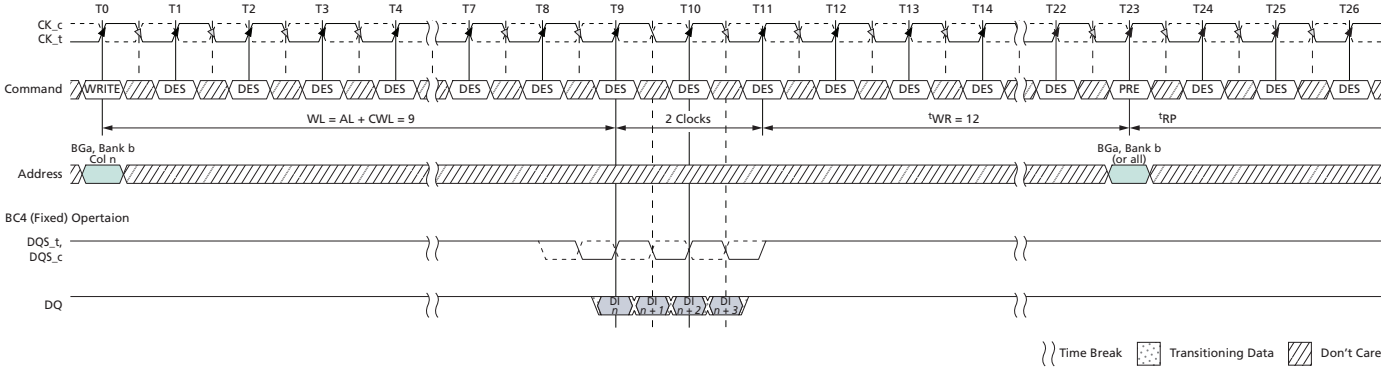
Figure 190: WRITE (BL8/BC4-OTF) to PRECHARGE with 1tCK Preamble



Notes: 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.

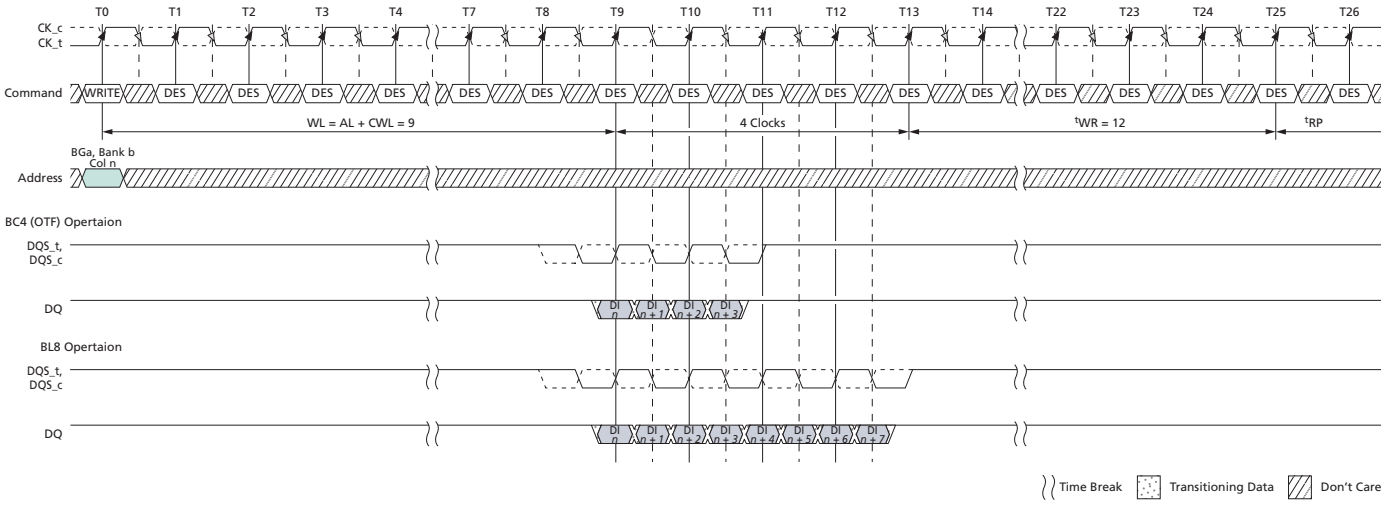
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at T13. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 191: WRITE (BC4-Fixed) to PRECHARGE with 1^{t}CK Preamble



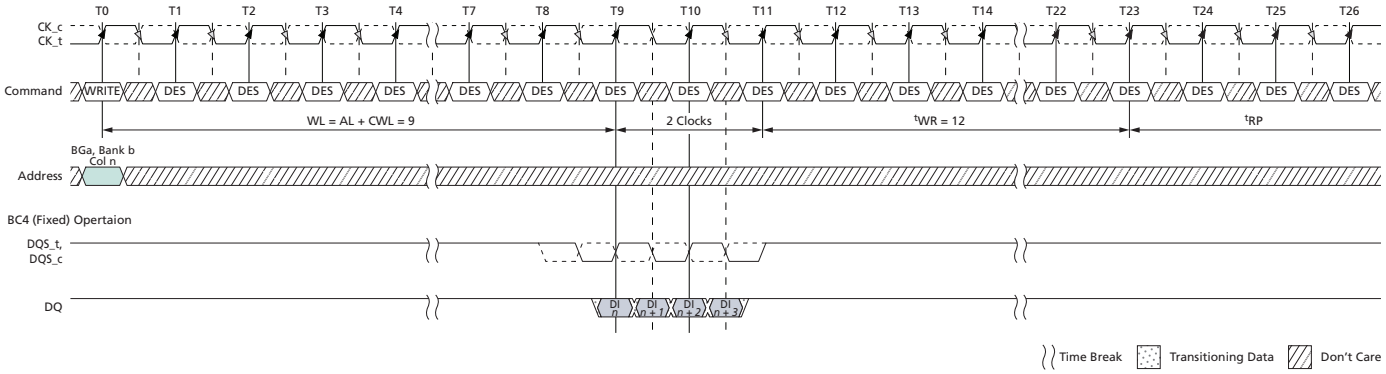
Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t}CK, ^{t}WR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at T11. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 192: WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1^{t}CK Preamble



Notes: 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t}CK, ^{t}WR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at T13. ^{t}WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

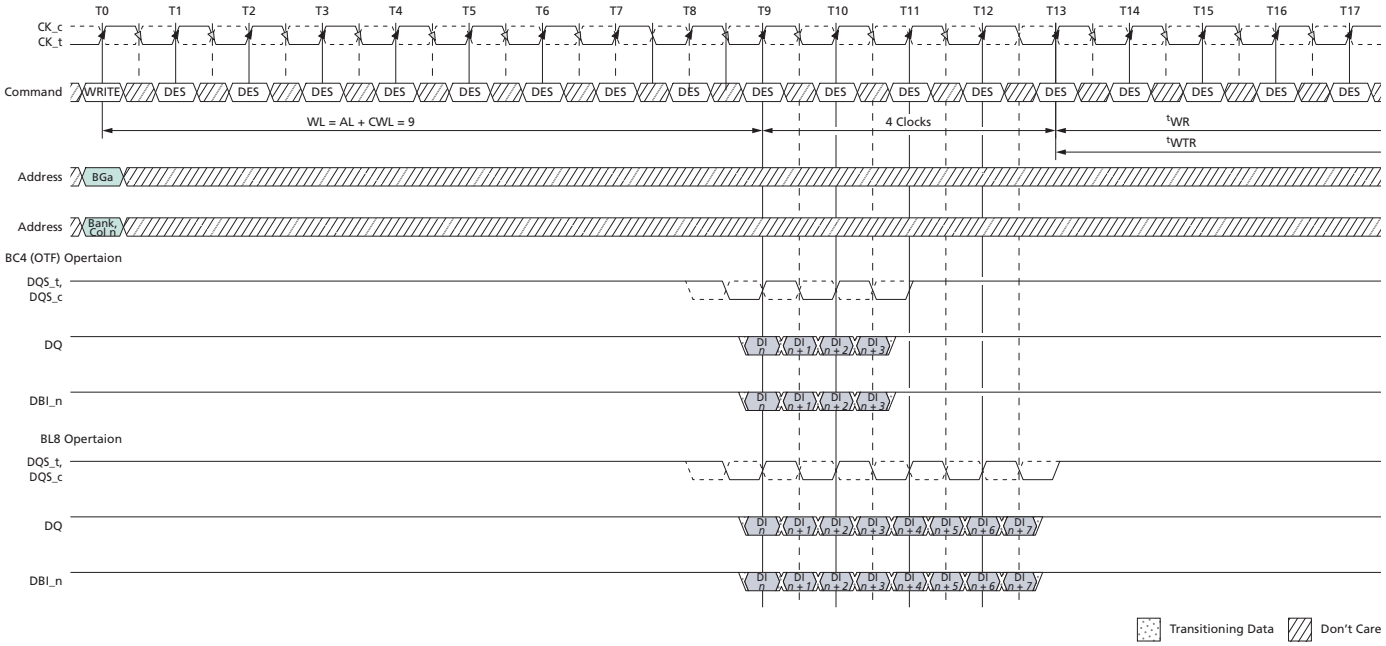
Figure 193: WRITE (BC4-Fixed) to Auto PRECHARGE with 1tCK Preamble



Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

WRITE Operation with WRITE DBI Enabled

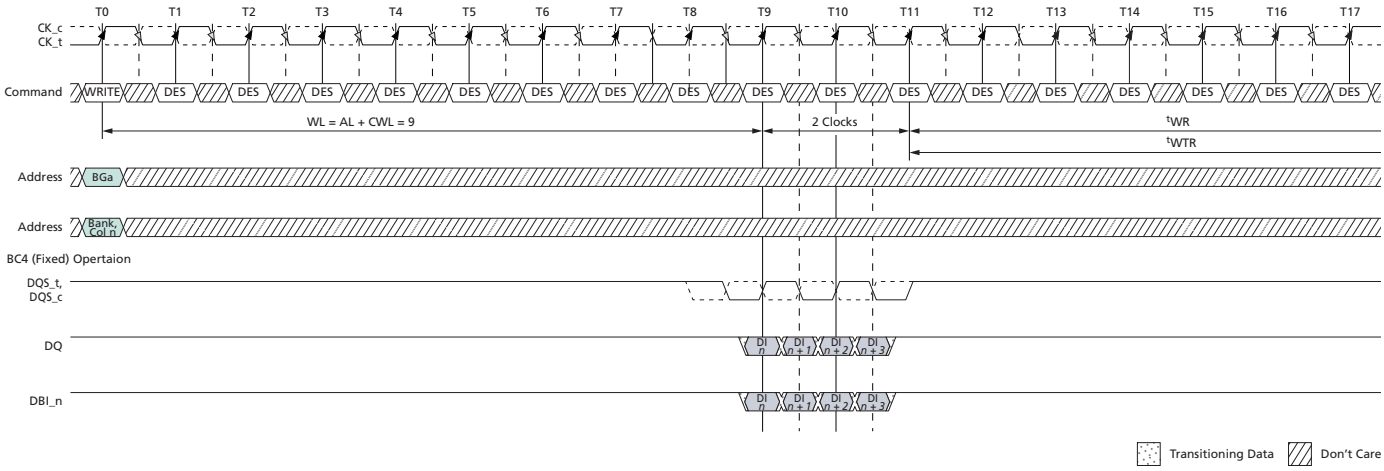
Figure 194: WRITE (BL8/BC4-OTF) with 1tCK Preamble and DBI



Notes: 1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.

6. The write recovery time (^{t}WR_DBI) is referenced from the first rising clock edge after the last write data shown at T13.

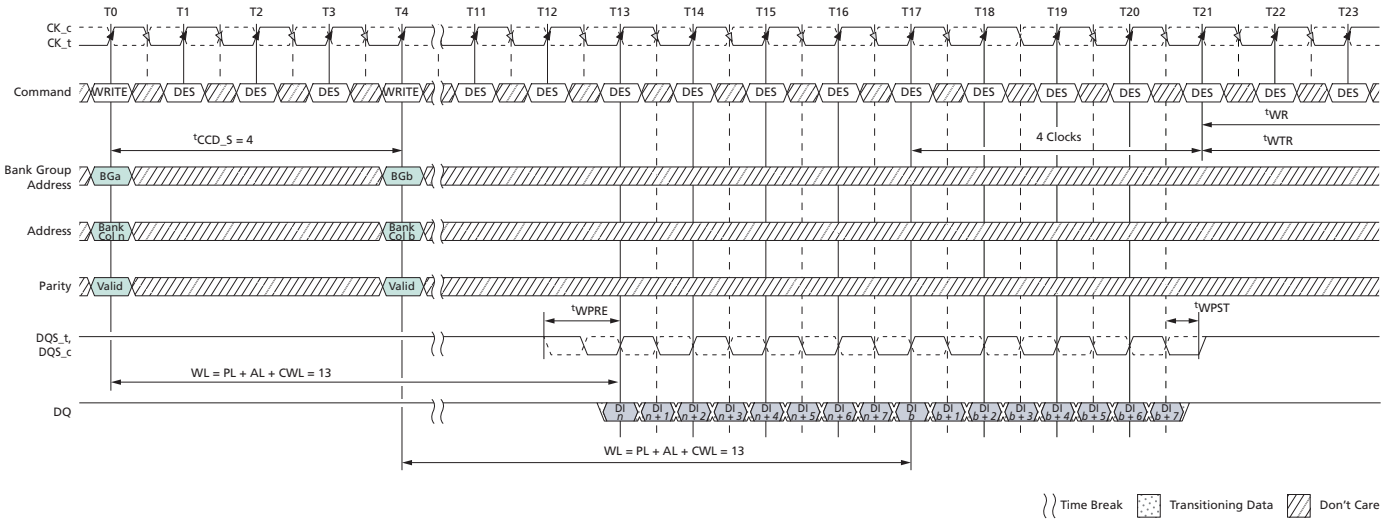
Figure 195: WRITE (BC4-Fixed) with 1^{t}CK Preamble and DBI



Notes: 1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t}CK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.

WRITE Operation with CA Parity Enabled

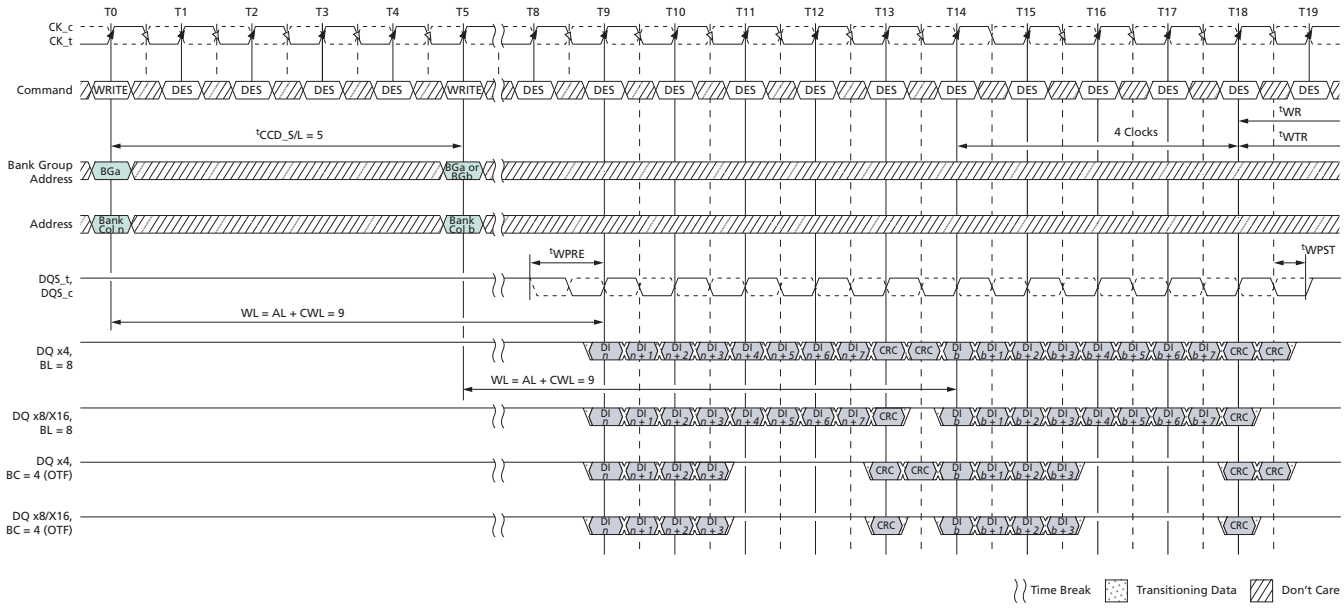
Figure 196: Consecutive Write (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



Notes: 1. BL = 8, WL = 9 (CWL = 13, AL = 0), Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Enable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

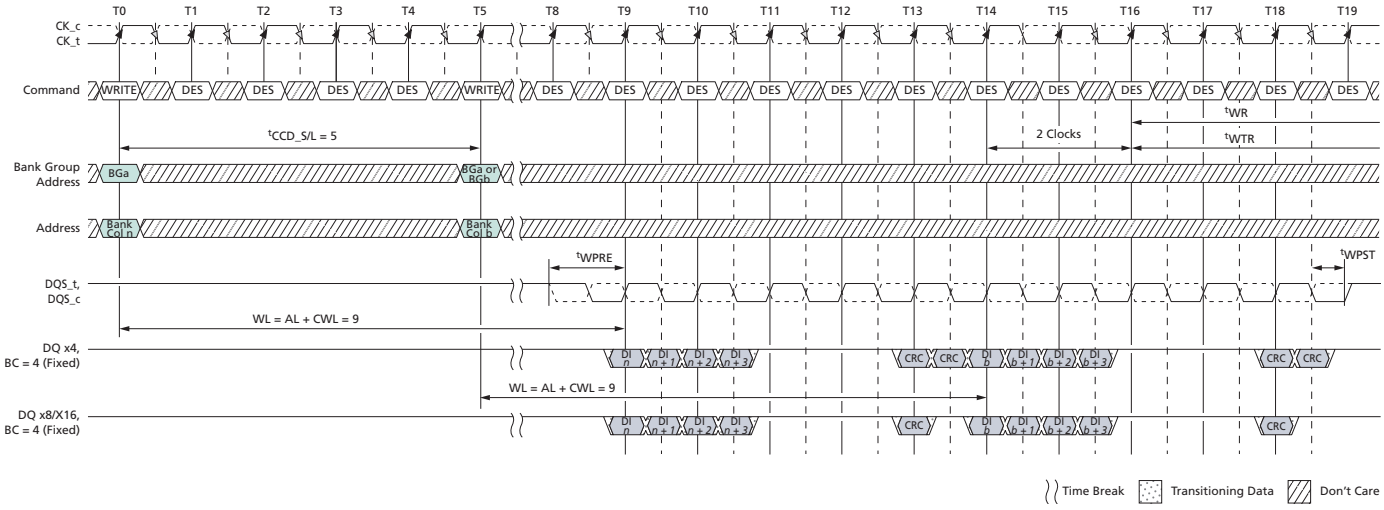
WRITE Operation with Write CRC Enabled

Figure 197: Consecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



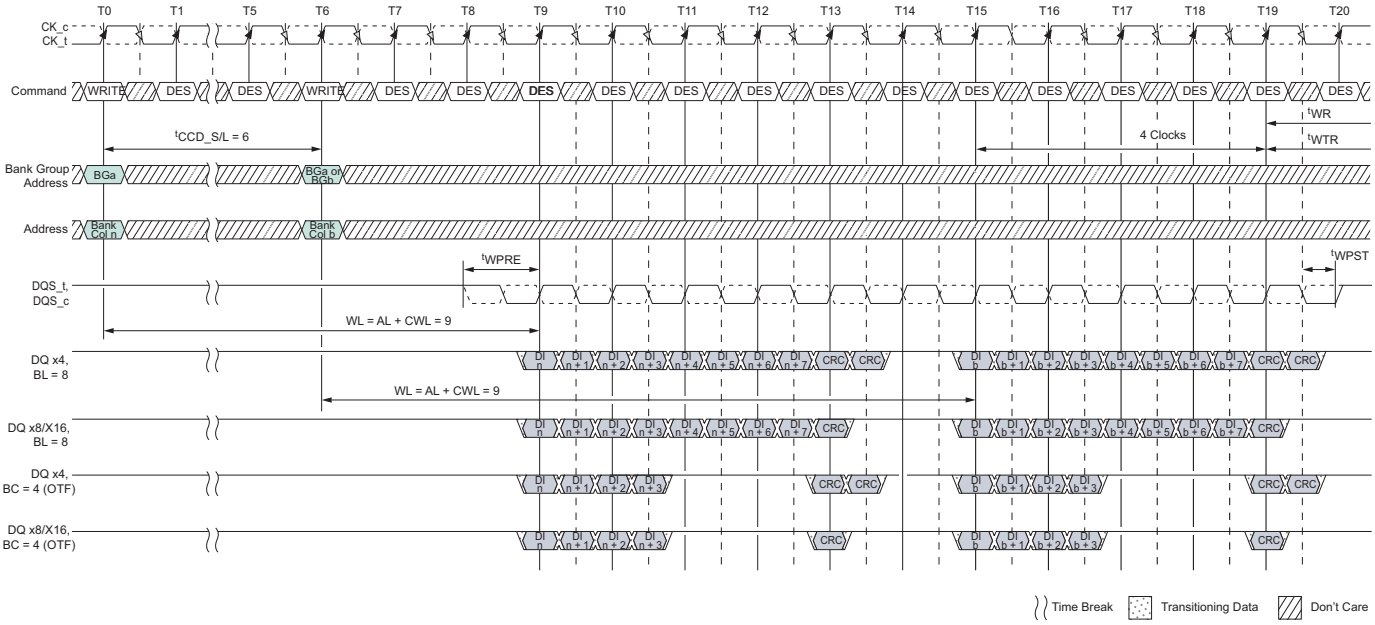
Notes: 1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T5.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Figure 198: Consecutive WRITE (BC4-Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



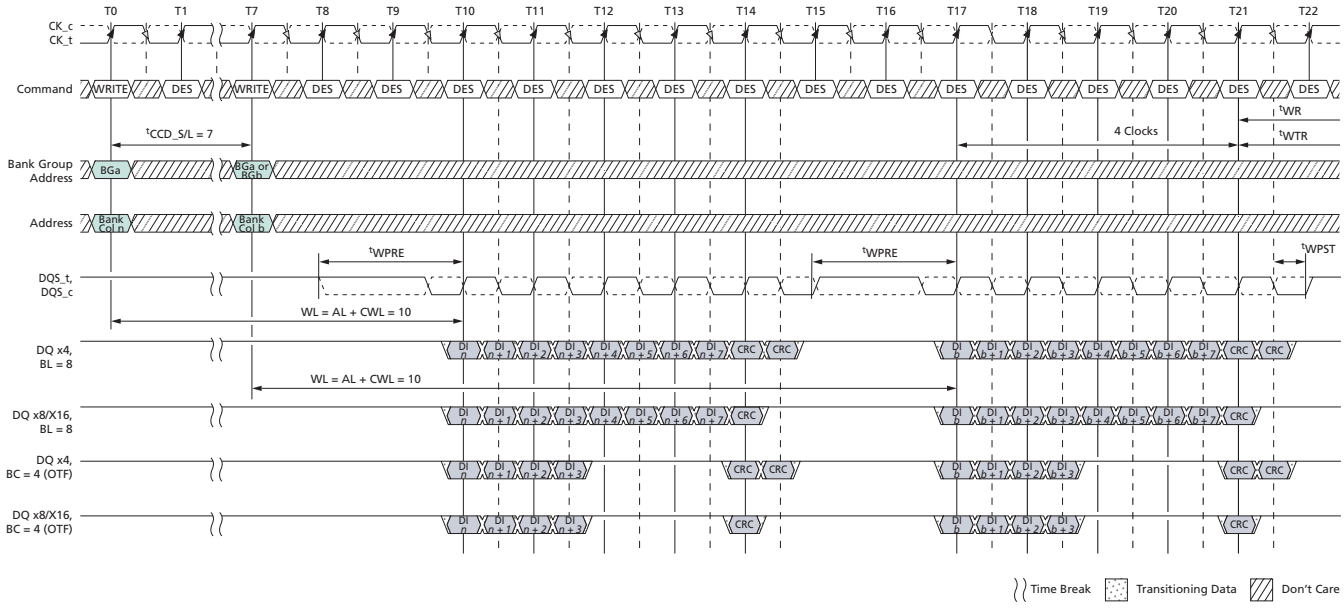
Notes: 1. BC4-fixed, AL = 0, CWL = 9, Preamble = 1^{t}CK, ^{t}CCD_S/L = 5^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10 during WRITE commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T16.

Figure 199: Nonconsecutive WRITE (BL8/BC4-OTF) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group



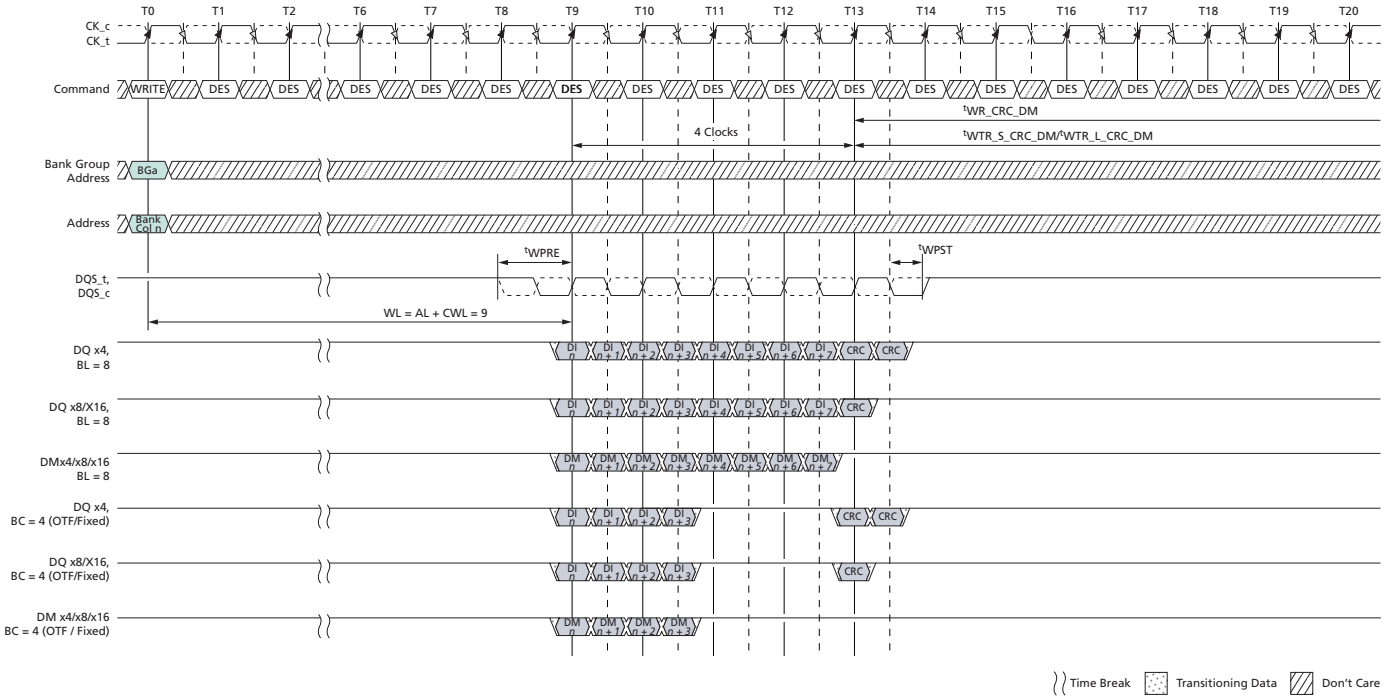
Notes: 1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1^{t}CK, ^{t}CCD_S/L = 6^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T6.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T19.

Figure 200: Nonconsecutive WRITE (BL8/BC4-OTF) with 2tCK Preamble and Write CRC in Same or Different Bank Group



Notes: 1. BL8/BC4-OTF, AL = 0, CWL = 9 + 1 = 10 (see Note 9), Preamble = 2tCK, tCCD_S/L = 7tCK (see Note 7).
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T7.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T7.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. tCCD_S/L = 6tCK is not allowed in 2tCK preamble mode if minimum tCCD_S/L allowed in 1tCK preamble mode would have been 6 clocks.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK WRITE preamble mode.

Figure 201: WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Notes: 1. BL8/BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_DM) and write timing parameter (tWTR_S_CRC_DM/tWTR_L_CRC_DM) are referenced from the first rising clock edge after the last write data shown at T13.

Write Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the device works properly. However, for certain minor violations, it is desirable that the device is guaranteed not to "hang up" and that errors are limited to that specific operation. A minor violation does not include a major timing violation (for example, when a DQS strobe misses in the ^{t}DQSCK window).

For the following, it will be assumed that there are no timing violations with regard to the WRITE command itself (including ODT, and so on) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

If the data-to-strobe timing requirements (^{t}DS, ^{t}DH) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example, the relevant strobe edges for WRITE Burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, and T8.5.

Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise.

Strobe-to-Strobe and Strobe-to-Clock Violations

If the strobe timing requirements (^{t}DQSH, ^{t}DQSL, ^{t}WPRE, ^{t}WPST) or the strobe to clock timing requirements (^{t}DSS, ^{t}DSH, ^{t}DQSS) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise with the following constraints:

- Both write CRC and data burst OTF are disabled; timing specifications other than ^{t}DQSH, ^{t}DQSL, ^{t}WPRE, ^{t}WPST, ^{t}DSS, ^{t}DSH, ^{t}DQSS are not violated.
- The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the WRITE latency position.
- A READ command following an offending WRITE command from any open bank is allowed.
- One or more subsequent WR or a subsequent WRA (to same bank as offending WR) may be issued ^{t}CCD_L later, but incorrect data could be written. Subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
- One or more subsequent WR or a subsequent WRA (to a different bank group) may be issued ^{t}CCD_S later, but incorrect data could be written. Subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
- After one or more precharge commands (PRE or PREA) are issued to the device after an offending WRITE command and all banks are in precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank will be able to write correct data.

ZQ CALIBRATION Commands

A ZQ CALIBRATION command is used to calibrate DRAM R_{ON} and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization and a relatively smaller time to perform periodic calibrations.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, after calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM I/O, which is reflected as an updated output driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of ^{t}ZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of ^{t}ZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter ^{t}ZQCS. One ZQCS command can effectively correct a minimum of 0.5% (ZQ correction) of R_{ON} and R_{TT} impedance error within 64 *n*CK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (T_{drift_rate}) and voltage (V_{drift_rate}) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQ_{correction}}{(T_{sense} \times T_{drift\_rate}) + (V_{sense} \times T_{drift\_rate})}$$

Where T_{sense} = MAX($dR_{TT}dT$, $dR_{ON}dTM$) and V_{sense} = MAX($dR_{TT}dV$, $dR_{ON}dVM$) define the temperature and voltage sensitivities.

For example, if T_{sens} = 1.5%/°C, V_{sens} = 0.15%/mV, $T_{driftrate}$ = 1 °C/sec and $V_{driftrate}$ = 15 mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

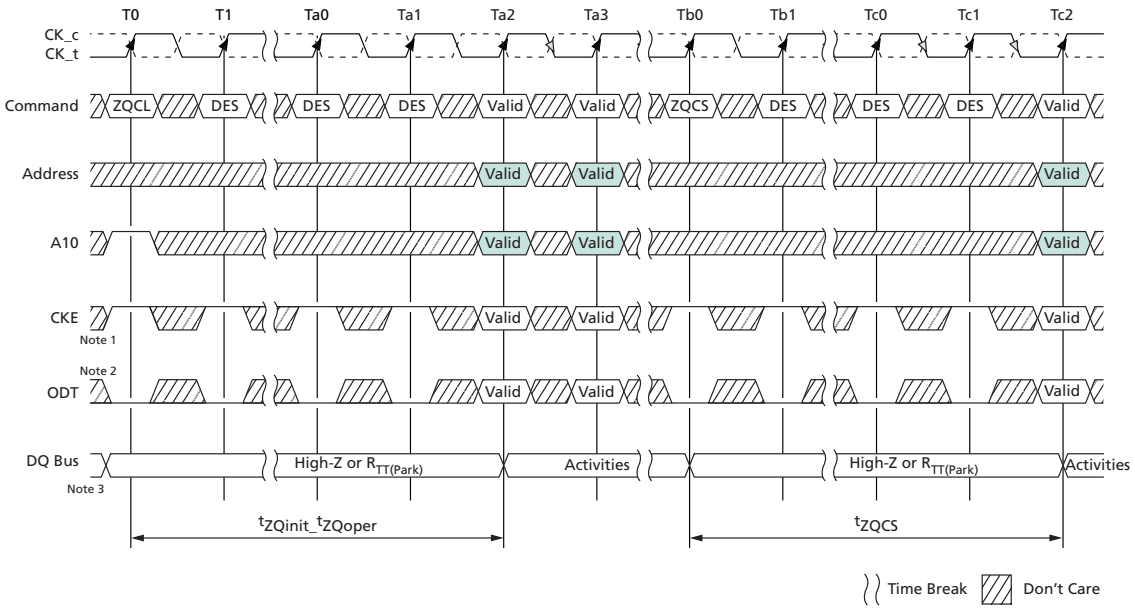
No other activities should be performed on the DRAM channel by the controller for the duration of ^{t}ZQinit, ^{t}ZQoper, or ^{t}ZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. After DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and ^{t}RP met before ZQCL or ZQCS commands are issued by the controller.

ZQ CALIBRATION commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an I/O calibration without an explicit ZQ CALIBRATION command. The earliest possible time for a ZQ CALIBRATION command (short or long) after self refresh exit is ^{t}XS, ^{t}XS_Abort, or ^{t}XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of ^{t}ZQoper, ^{t}ZQinit, or ^{t}ZQCS between the devices.

Figure 202: ZQ Calibration Timing



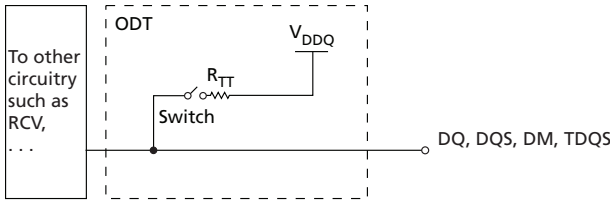
Notes: 1. CKE must be continuously registered HIGH during the calibration procedure.
2. During ZQ calibration, the ODT signal must be held LOW and DRAM continues to provide RTT_PARK.
3. All devices connected to the DQ bus should be High-Z during the calibration procedure.

On-Die Termination

The on-die termination (ODT) feature enables the device to change termination resistance for each DQ, DQS, and DM_n/DBI_n signal for x4 and x8 configurations (and TDQS for the x8 configuration when enabled via A11 = 1 in MR1) via the ODT control pin, WRITE command, or default parking value with MR setting. For the x16 configuration, ODT is applied to each UDQ, LDQ, UDQS, LDQS, UDM_n/UDBI_n, and LDM_n/LDBI_n signal. The ODT feature is designed to improve the signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. If DBI read mode is enabled while the DRAM is in standby, either DM mode or DBI write mode must also be enabled if $R_{TT(NOM)}$ or $R_{TT(Park)}$ is desired. More details about ODT control modes and ODT timing modes can be found further along in this document.

The ODT feature is turned off and not supported in self refresh mode.

Figure 203: Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of R_{TT} is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable $R_{TT(NOM)}$ [MR1[10,9,8] = 0,0,0] and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT mode of the DDR4 device has four states: data termination disable, $R_{TT(NOM)}$, $R_{TT(WR)}$, and $R_{TT(Park)}$. The ODT mode is enabled if any of MR1[10:8] ($R_{TT(NOM)}$), MR2[11:9] ($R_{TT(WR)}$), or MR5[8:6] ($R_{TT(Park)}$) are non-zero. When enabled, the value of R_{TT} is determined by the settings of these bits.

R_{TT} control of each R_{TT} condition is possible with a WR or RD command and ODT pin.

- $R_{TT(WR)}$: The DRAM (rank) that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).
- $R_{TT(NOM)}$: DRAM turns ON $R_{TT(NOM)}$ if it sees ODT asserted HIGH (except when ODT is disabled by MR1).
- $R_{TT(Park)}$: Default parked value set via MR5 to be enabled and $R_{TT(NOM)}$ is not turned on.
- The Termination State Table that follows shows various interactions.

The R_{TT} values have the following priority:

- Data termination disable
- $R_{TT(WR)}$
- $R_{TT(NOM)}$
- $R_{TT(Park)}$

Table 72: Termination State Table

Case	$R_{TT(Park)}$	$R_{TT(NOM)}$ [1]	$R_{TT(WR)}$ [2]	ODT Pin	ODT READS[3]	ODT Standby[7]	ODT WRITES
A[4]	Disabled	Disabled	Disabled	Don't Care	Off (High-Z)	Off (High-Z)	Off (High-Z)
			Enabled	Don't Care	Off (High-Z)	Off (High-Z)	$R_{TT(WR)}$
B[5]	Enabled	Disabled	Disabled	Don't Care	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(Park)}$
			Enabled	Don't Care	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(WR)}$
C[6]	Disabled	Enabled	Disabled	Low	Off (High-Z)	Off (High-Z)	Off (High-Z)
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(NOM)}$
			Enabled	Low	Off (High-Z)	Off (High-Z)	$R_{TT(WR)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(WR)}$
D[6]	Enabled	Enabled	Disabled	Low	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(Park)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(NOM)}$
			Enabled	Low	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(WR)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(WR)}$

Notes: 1. If $R_{TT(NOM)}$ MR is disabled, power to the ODT receiver will be turned off to save power.
2. If $R_{TT(WR)}$ is enabled, $R_{TT(WR)}$ will be activated by a WRITE command for a defined period time independent of the ODT pin and MR setting of $R_{TT(Park)}$/$R_{TT(NOM)}$. This is described in the Dynamic ODT section.
3. When a READ command is executed, the DRAM termination state will be High-Z for a defined period independent of the ODT pin and MR setting of $R_{TT(Park)}$/$R_{TT(NOM)}$. This is described in the ODT During Read section.
4. Case A is generally best for single-rank memories.
5. Case B is generally best for dual-rank, single-slotted memories.
6. Case C and Case D are generally best for multi-slotted memories.
7. The ODT feature is turned off and not supported in self refresh mode.

ODT Read Disable State Table

Upon receiving a READ command, the DRAM driving data disables ODT after RL - (2 or 3) clock cycles, where 2 = 1^{t}CK preamble mode and 3 = 2^{t}CK preamble mode. ODT stays off for a duration of BL/2 + (2 or 3) + (0 or 1) clock cycles, where 2 = 1^{t}CK preamble mode, 3 = 2^{t}CK preamble mode, 0 = CRC disabled, and 1 = CRC enabled.

Table 73: Read Termination Disable Window

Preamble	CRC	Start ODT Disable After Read	Duration of ODT Disable
1^{t}CK	Disabled	RL - 2	BL/2 + 2
	Enabled	RL - 2	BL/2 + 3
2^{t}CK	Disabled	RL - 3	BL/2 + 3
	Enabled	RL - 3	BL/2 + 4

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes include the following:

- Any bank active with CKE HIGH
- Refresh with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode
- Precharge power-down mode

In synchronous ODT mode, $R_{TT(NOM)}$ will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is determined by the programmed values for: CAS WRITE latency (CWL), additive latency (AL), and parity latency (PL), as well as the programmed state of the preamble.

ODT Latency and Posted ODT

The ODT latencies for synchronous ODT mode are summarized in the table below. For details, refer to the latency definitions.

Table 74: ODT Latency at DDR4-1600/-1866/-2133/-2400/-2666/-3200

Applicable when write CRC is disabled

Symbol	Parameter	1^{t}CK Preamble	2^{t}CK Preamble	Unit
DODTLon	Direct ODT turn-on latency	CWL + AL + PL - 2	CWL + AL + PL - 3	^{t}CK
DODTLoff	Direct ODT turn-off latency	CWL + AL + PL - 2	CWL + AL + PL - 3	
RODTLoff	READ command to internal ODT turn-off latency	CL + AL + PL - 2	CL + AL + PL - 3	
RODTLon4	READ command to $R_{TT(Park)}$ turn-on latency in BC4-fixed	RODTLoff + 4	RODTLoff + 5	
RODTLon8	READ command to $R_{TT(Park)}$ turn-on latency in BL8/BC4-OTF	RODTLoff + 6	RODTLoff + 7	
ODTH4	ODT Assertion time, BC4 mode	4	5	
ODTH8	ODT Assertion time, BL8 mode	6	7	

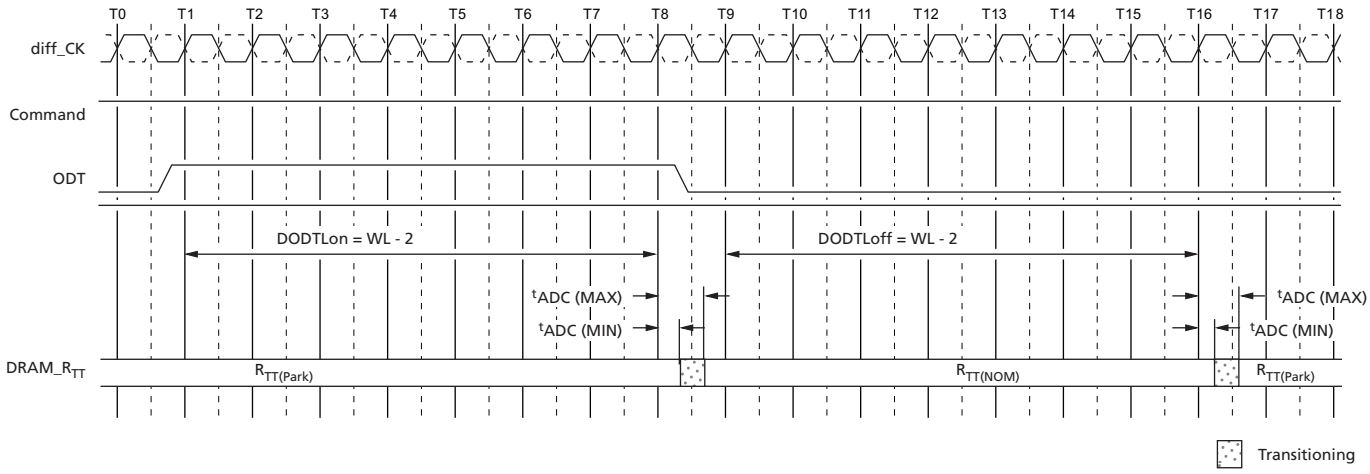
Timing Parameters

In synchronous ODT mode, the following parameters apply:

- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, and ^{t}ADC (MIN)/(MAX).
- ^{t}ADC (MIN) and ^{t}ADC (MAX) are minimum and maximum R_{TT} change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

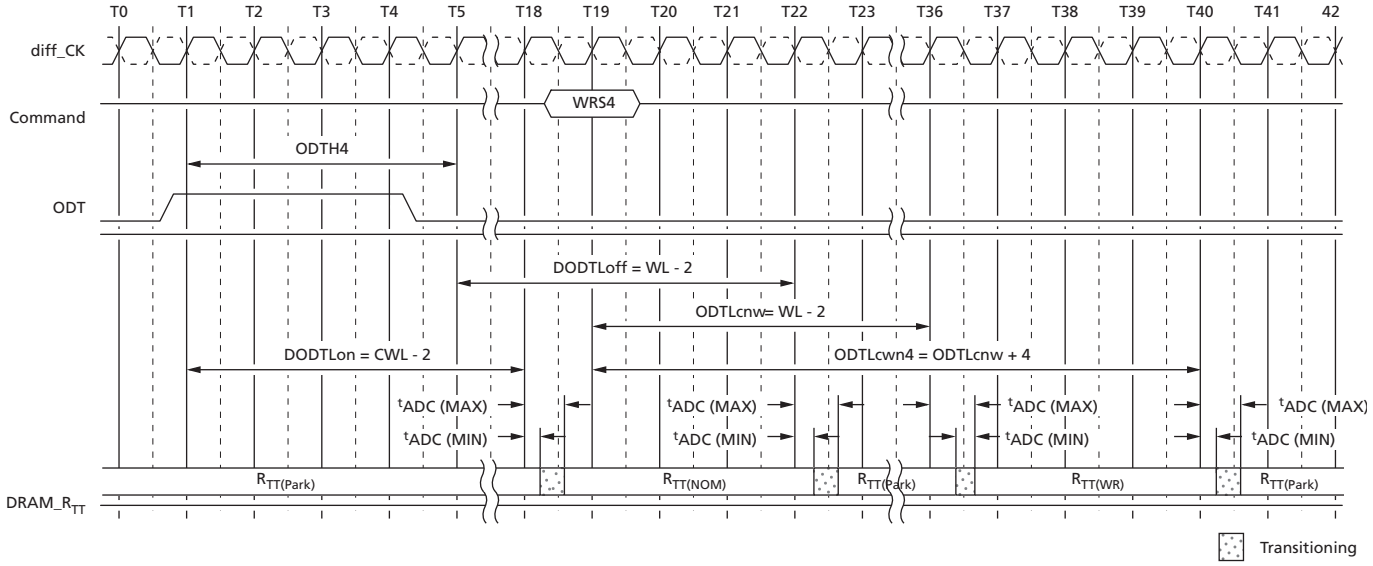
When ODT is asserted, it must remain HIGH until minimum ODTH4 (BC = 4) or ODTH8 (BL = 8) is satisfied. If write CRC mode or 2^{t}CK preamble mode is enabled, ODTH should be adjusted to account for it. ODTH*x* is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of a WRITE command.

Figure 204: Synchronous ODT Timing with BL8



Notes: 1. Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL + CWL - 2 = 7; DODTLoff = AL + PL + CWL - 2 = 7.
2. ODT must be held HIGH for at least ODTH8 after assertion (T1).

Figure 205: Synchronous ODT with BC4



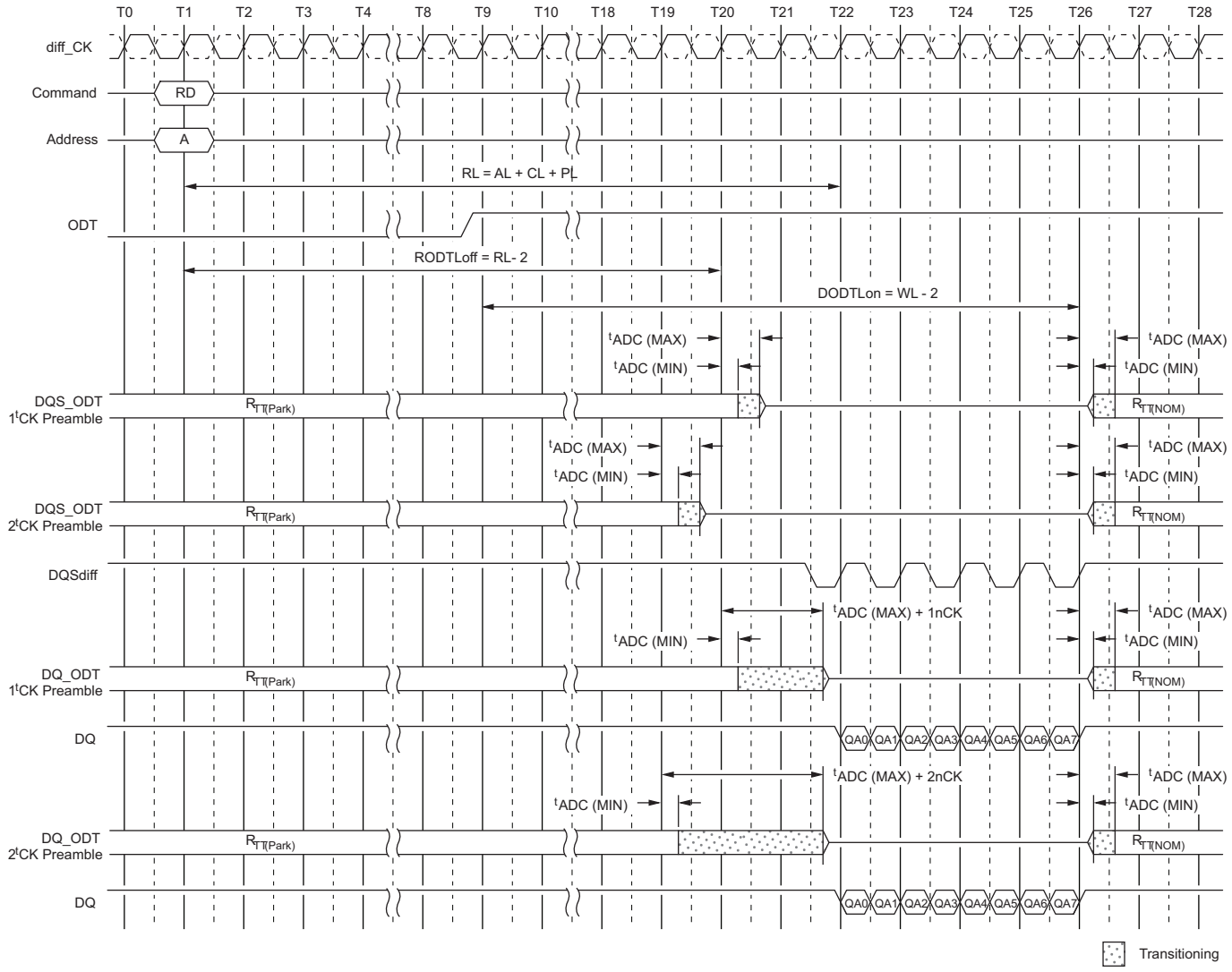
Notes: 1. Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL+ CWL - 2 = 17; ODTcnw = AL + PL+ CWL - 2 = 17.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).

ODT During Reads

Because the DRAM cannot terminate with R_{TT} and drive with R_{ON} at the same time, R_{TT} may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T26 the device turns on the termination when it stops driving, which is determined by ^{t}HZ. If the DRAM stops driving early (that is, ^{t}HZ is early), then^{t}ADC (MIN) timing may apply. If the DRAM stops driving late (that is, ^{t}HZ is late), then the DRAM complies with ^{t}ADC (MAX) timing.

Using CL = 11 as an example for the figure below: PL = 0, AL = CL - 1 = 10, RL = PL + AL + CL = 21, CWL= 9; RODTLoff = RL - 2 = 19, DODTLon = PL + AL + CWL - 2 = 17, 1^{t}CK preamble.

Figure 206: ODT During Reads



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature.

Functional Description

Dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three R_{TT}values are available: $R_{TT(NOM)}$, $R_{TT(WR)}$, and $R_{TT(Park)}$.
  - The value for $R_{TT(NOM)}$ is preselected via bits MR1[10:8].
  - The value for $R_{TT(WR)}$ is preselected via bits MR2[11:9].
  - The value for $R_{TT(Park)}$ is preselected via bits MR5[8:6].
- During operation without WRITE commands, the termination is controlled as follows:
  - Nominal termination strength $R_{TT(NOM)}$ or $R_{TT(Park)}$ is selected.
  - $R_{TT(NOM)}$ on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff, and $R_{TT(Park)}$ is on when ODT is LOW.
- When a WRITE command (WR, WRA, WRS4, WRS8, WRAS4, and WRAS8) is registered, and if dynamic ODT is enabled, the termination is controlled as follows:
  - Latency ODTLcnw after the WRITE command, termination strength $R_{TT(WR)}$ is selected.
  - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the WRITE command, termination strength $R_{TT(WR)}$ is de-selected.

One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC mode and/or 2^{t}CK preamble enablement.

The following table shows latencies and timing parameters relevant to the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. An MRS command must be used to set $R_{TT(WR)}$ to disable dynamic ODT externally (MR2[11:9] = 000).

Table 75: Dynamic ODT Latencies and Timing (1^{t}CK Preamble Mode and CRC Disabled)

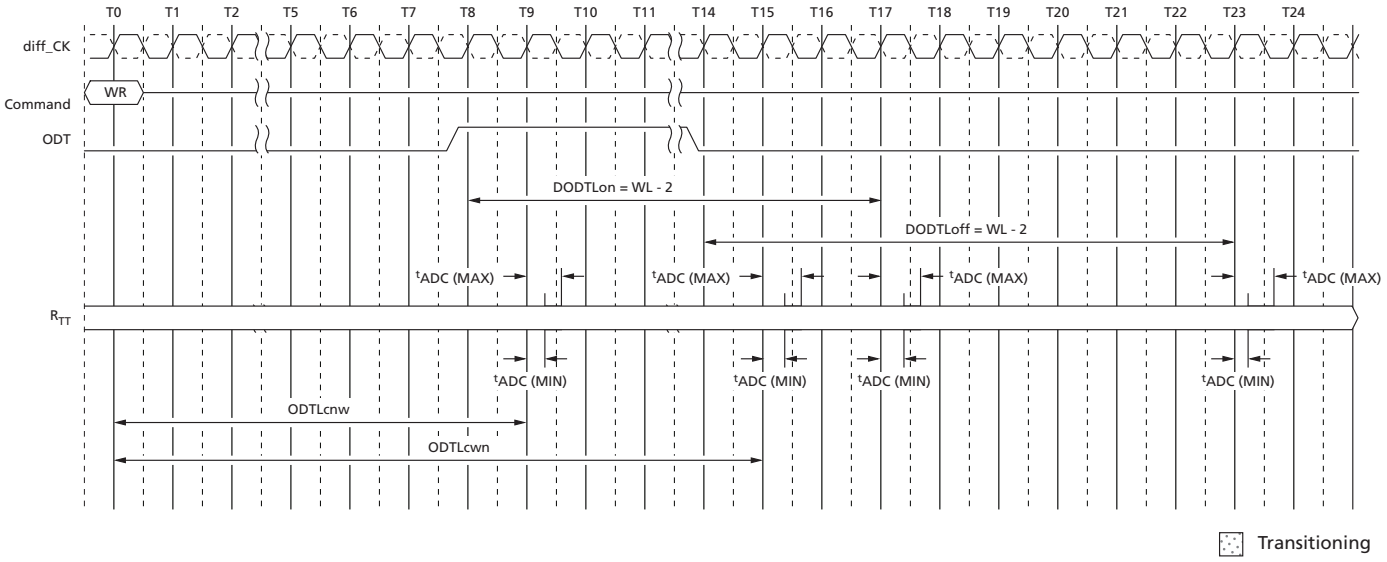
Name and Description	Abbr.	Defined from	Defined to	1600/1866/2133/2400	2666	2933/3200	Unit
ODT latency for change from $R_{TT(Park)}$/$R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcnw	Registering external WRITE command	Change R_{TT} strength from $R_{TT(Park)}$/$R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcnw = WL - 2			^{t}CK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$ (BC = 4)	ODTLcwn4	Registering external WRITE command	Change R_{TT} strength from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$	ODTLcwn4 = 4 + ODTLcnw			^{t}CK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$ (BL = 8)	ODTLcwn8	Registering external WRITE command	Change R_{TT} strength from $R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcwn8 = 6 + ODTLcnw			^{t}CK (AVG)
R_{TT} change skew	^{t}ADC	ODTLcnw ODTLcwn	R_{TT} valid	^{t}ADC (MIN) = 0.30 ^{t}ADC (MAX) = 0.70	^{t}ADC (MIN) = 0.28 ^{t}ADC (MAX) = 0.72	^{t}ADC (MIN) = 0.26 ^{t}ADC (MAX) = 0.74	^{t}CK (AVG)

Table 76: Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix

Symbol	1tCK Parameter		2tCK Parameter		Unit
	CRC Off	CRC On	CRC Off	CRC On	
ODTLcnw[1]	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw + 4	ODTLcnw + 7	ODTLcnw + 5	ODTLcnw + 8	
ODTLcwn8	ODTLcnw + 6	ODTLcnw + 7	ODTLcnw + 7	ODTLcnw + 8	

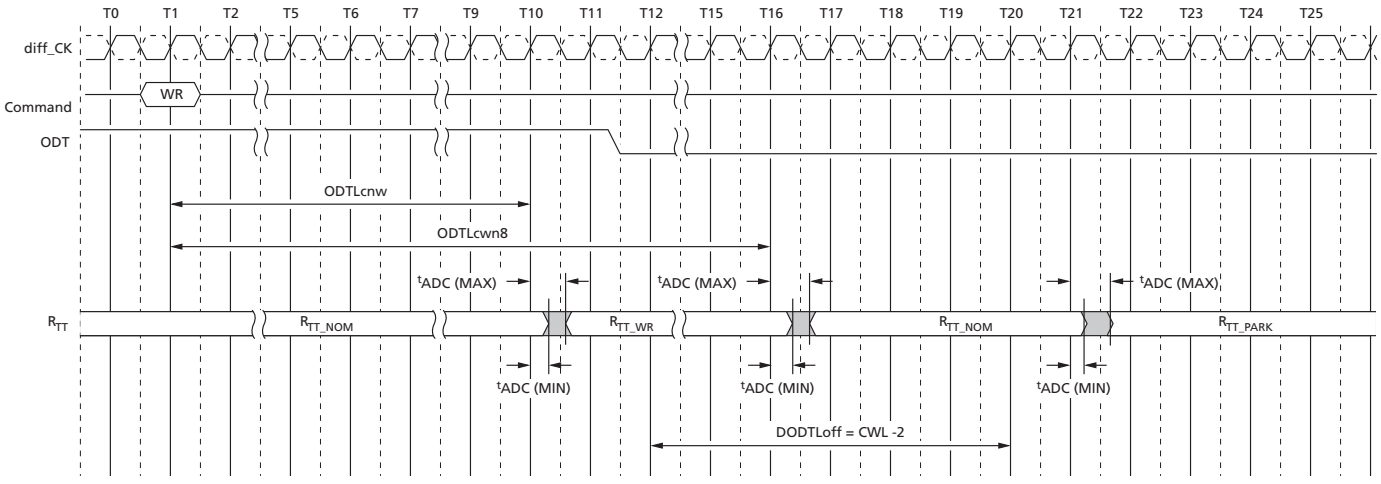
Notes: 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).

Figure 207: Dynamic ODT (1t CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



Notes: 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).
2. If BC4, then ODTLcwn = WL + 4 if CRC disabled or WL + 5 if CRC enabled; If BL8, then ODTLcwn = WL + 6 if CRC disabled or WL + 7 if CRC enabled.

Figure 208: Dynamic ODT Overlapped with $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



Note: 1. Behavior with WR command issued while ODT is registered HIGH.

Asynchronous ODT Mode

Asynchronous ODT mode is selected when the DRAM runs in DLL-off mode. In asynchronous ODT timing mode, the internal ODT command is *not* delayed by either additive latency (AL) or the parity latency (PL) relative to the external ODT signal ($R_{TT(NOM)}$). In asynchronous ODT mode, two timing parameters apply: ^{t}AONAS (MIN/MAX), and ^{t}AOFAS (MIN/MAX).

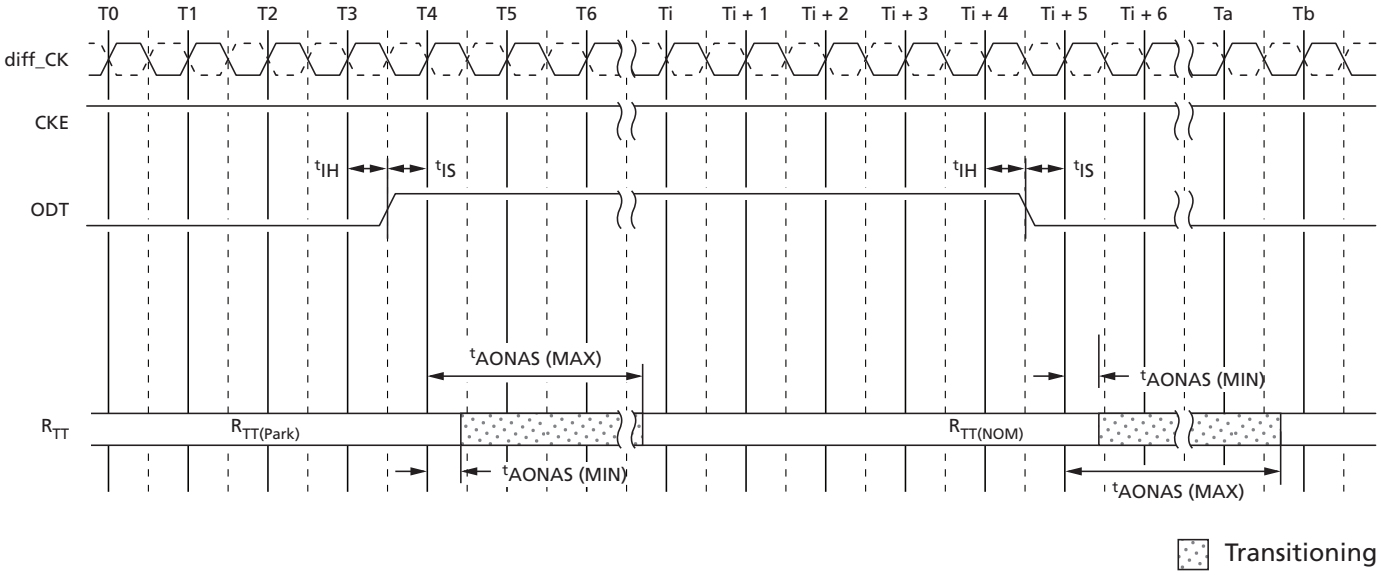
$R_{TT(NOM)}$ Turn-on Time

- Minimum $R_{TT(NOM)}$ turn-on time (^{t}AONAS [MIN]) is when the device termination circuit leaves $R_{TT(Park)}$ and ODT resistance begins to turn on.
- Maximum $R_{TT(NOM)}$ turn-on time (^{t}AONAS [MAX]) is when the ODT resistance has reached $R_{TT(NOM)}$.
- ^{t}AONAS (MIN) and ^{t}AONAS (MAX) are measured from ODT being sampled HIGH.

$R_{TT(NOM)}$ Turn-off Time

- Minimum $R_{TT(NOM)}$ turn-off time (^{t}AOFAS [MIN]) is when the device's termination circuit starts to leave $R_{TT(NOM)}$.
- Maximum $R_{TT(NOM)}$ turn-off time (^{t}AOFAS [MAX]) is when the on-die termination has reached $R_{TT(Park)}$.
- ^{t}AOFAS (MIN) and ^{t}AOFAS (MAX) are measured from ODT being sampled LOW.

Figure 209: Asynchronous ODT Timings with DLL Off



Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability. Although "unlimited" row accesses to the same row is allowed within the refresh period; excessive row accesses to the same row over a long term can result in degraded operation.

Table 77: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	
T_{STG}	Storage temperature	–55	150	°C	2

Notes: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to the JESD51-2 standard.
3. V_{PP} must be equal to or greater than V_{DD}/V_{DDQ} at all times when powered.

DRAM Component Operating Temperature Range

Operating temperature, T_{OPER}, is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JEDEC document JESD51-2.

Table 78: Temperature Range

Symbol	Parameter	Min	Max	Unit	Notes
T_{OPER}	Normal operating temperature range	-40	85	°C	1
	Extended temperature range (optional)	>85	105	°C	2

Notes: 1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The industrial and automotive temperature offerings allow the case temperature to go below 0°C to -40°C.
2. Some applications require operation of the commercial, industrial, and automotive temperature DRAMs in the extended temperature range (between 85°C and 105°C case temperature). Full specifications are supported in this range, but the following additional conditions apply:
   - Refer to tREFI and tRFC parameters table for tREFI requirements when operating above 85°C
   - If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range capability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

Electrical Characteristics – AC and DC Operating Conditions

Supply Operating Conditions

Table 79: Recommended Supply Operating Conditions

Symbol	Parameter	Rating			Unit	Notes
		Min	Typ	Max		
V_{DD}	Supply voltage	1.14	1.2		1.26V	1, 2, 3, 4, 5
V_{DDQ}	Supply voltage for output	1.14	1.2		1.26V	1, 2, 6
V_{PP}	Wordline supply voltage	2.375	2.5		2.750V	7

Notes: 1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. V_{DD} slew rate between 300mV and 80% of $V_{DD,min}$ shall be between 0.004 V/ms and 600 V/ms, 20 MHz band-limited measurement.
4. V_{DD} ramp time from 300mV to $V_{DD,min}$ shall be no longer than 200ms.
5. A stable valid V_{DD} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DD} provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.
6. A stable valid V_{DDQ} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.
7. A stable valid V_{PP} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±120mV (greater than 250 KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.

Table 80: V_{DD} Slew Rate

Symbol	Min	Max	Unit	Notes
V_{DD_sl}	0.004	600	V/ms	1, 2
V_{DD_on}	–	200	ms	3

Notes: 1. Measurement made between 300mV and 80% V_{DD} (minimum level).
2. The DC bandwidth is limited to 20 MHz.
3. Maximum time to ramp V_{DD} from 300 mV to V_{DD} minimum.

Leakages

Table 81: Leakages

Condition	Symbol	Min	Max	Unit	Notes
Input leakage (excluding ZQ and TEN)	I_{IN}	–2	2	µA	1
ZQ leakage	I_{ZQ}	–50	10	µA	1
TEN leakage	I_{TEN}	–6	10	µA	1, 2
V_{REFCA} leakage	I_{VREFCA}	–2	2	µA	3
Output leakage: $V_{OUT} = V_{DDQ}$	I_{OZpd}	–	10	µA	4
Output leakage: $V_{OUT} = V_{SSQ}$	I_{OZpu}	–50	–	µA	4, 5

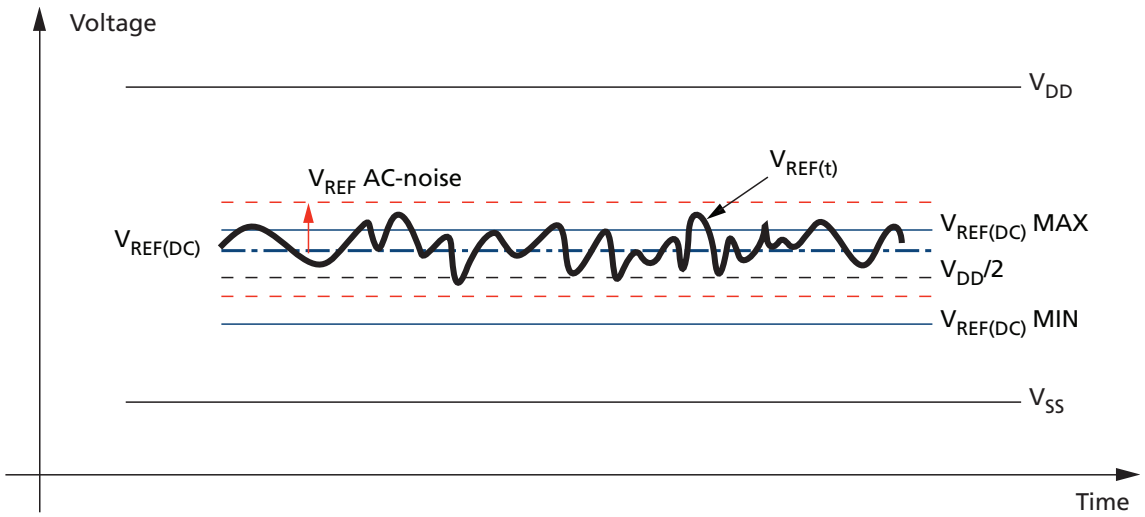
Notes: 1. Input under test $0V < V_{IN} < 1.1V$.
2. Additional leakage due to weak pull-down.
3. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level after initialization.
4. DQs are disabled.
5. ODT is disabled with the ODT input HIGH.

V_{REFCA} Supply

V_{REFCA} is to be supplied to the DRAM and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{REF(t)}$ as a function of time (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ±1% V_{DD} for the AC-noise limit.

Figure 210: V_{REFDQ} Voltage Range



The voltage levels for setup and hold time measurements are dependent on V_{REF}. V_{REF} is understood as $V_{REF(DC)}$, as defined in the above figure. This clarifies that DC-variations of V_{REF} affect the absolute

voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (±1% of V_{DD}) are included in DRAM timings and their associated deratings.

V_{REFDQ} Supply and Calibration Ranges

The device internally generates its own V_{REFDQ}. DRAM internal V_{REFDQ} specification parameters: voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level are used to help provide estimated values for the internal V_{REFDQ} and are not pass/fail limits. The voltage operating range specifies the minimum required range for DDR4 SDRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. A calibration sequence should be performed by the DRAM controller to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers.

Table 82: V_{REFDQ} Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Range 1 V_{REFDQ} operating points	V_{REFDQ} R1	60%	–	92%	V_{DDQ}	1, 2
Range 2 V_{REFDQ} operating points	V_{REFDQ} R2	45%	–	77%	V_{DDQ}	1, 2
V_{REF} step size	$V_{REF,step}$	0.5%	0.65%	0.8%	V_{DDQ}	3
V_{REF} set tolerance	V_{REF,set_tol}	–1.625%	0%	1.625%	V_{DDQ}	4, 5, 6
		–0.15%	0%	0.15%	V_{DDQ}	4, 7, 8
V_{REF} step time	$V_{REF,time}$	–	–	150	ns	9, 10, 11
V_{REF} valid tolerance	$V_{REF\_val\_tol}$	–0.15%	0%	0.15%	V_{DDQ}	12

Notes:
1. $V_{REF(DC)}$ voltage is referenced to $V_{DDQ(DC)}$. $V_{DDQ(DC)}$ is 1.2V.
2. DRAM range 1 or range 2 is set by the MRS6[6]6.
3. V_{REF} step size increment/decrement range. V_{REF} at DC level.
4. $V_{REF,new} = V_{REF,old} \pm n \times V_{REF,step}$; n = number of steps. If increment, use "+," if decrement, use "-."
5. For n >4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ - 1.625% × V_{DDQ}. The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 1.625% × V_{DDQ}.
6. Measured by recording the MIN and MAX values of the V_{REF} output over the range, drawing a straight line between those points, and comparing all other V_{REF} output settings to that line.
7. For n ≤4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ - 0.15% × V_{DDQ}. The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 0.15% × V_{DDQ}.
8. Measured by recording the MIN and MAX values of the V_{REF} output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all V_{REF} output settings to that line.
9. Time from MRS command to increment or decrement one step size for V_{REF}.
10. Time from MRS command to increment or decrement more than one step size up to the full range of V_{REF}.
11. If the V_{REF} monitor is enabled, V_{REF} must be derated by +10ns if DQ bus load is 0pF and an additional +15 ns/pF of DQ bus loading.
12. Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid qualifies the step times, which will be characterized at the component level.

V_{REFDQ} Ranges

MR6[6] selects range 1 (60% to 92.5% of V_{DDQ}) or range 2 (45% to 77.5% of V_{DDQ}), and MR6[5:0] sets the V_{REFDQ} level, as listed in the following table. The values in MR6[6:0] will update the V_{DDQ} range and level independent of MR6[7] setting. It is recommended MR6[7] be enabled when changing the settings in MR6[6:0], and it is highly recommended MR6[7] be enabled when changing the settings in MR6[6:0] multiple times during a calibration routine.

Table 83: V_{REFDQ} Range and Levels

MR6[5:0]	MR6[6] 0 = Range 1	MR6[6] 1 = Range 2	MR6[5:0]	MR6[6] 0 = Range 1	MR6[6] 1 = Range 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 are reserved		

Electrical Characteristics – AC and DC Single-Ended Input Measurement Levels

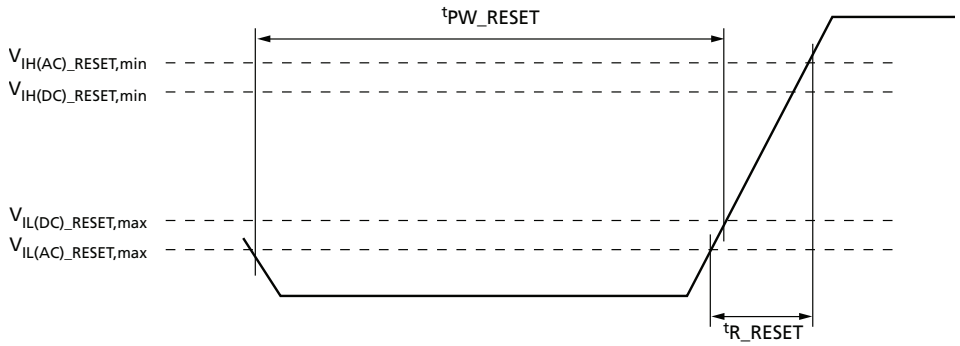
RESET_n Input Levels

Table 84: RESET_n Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)\_RESET}$	0.8 × V_{DD}	V_{DD}	V	1
DC input high voltage	$V_{IH(DC)\_RESET}$	0.7 × V_{DD}	V_{DD}	V	2
DC input low voltage	$V_{IL(DC)\_RESET}$	V_{SS}	0.3 × V_{DD}	V	3
AC input low voltage	$V_{IL(AC)\_RESET}$	V_{SS}	0.2 × V_{DD}	V	4
Rising time	$^{t}R\_RESET$	–	1	µs	5
RESET pulse width after power-up	$^{t}PW\_RESET\_S$	1	–	µs	6, 7
RESET pulse width during power-up	$^{t}PW\_RESET\_L$	200	–	µs	6

Notes: 1. Overshoot should not exceed the V_{IN} shown in the Absolute Maximum Ratings table.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above $V_{IH(DC)\_RESET}$, otherwise operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. After RESET_n is registered LOW, the RESET_n level must be maintained below $V_{IL(DC)\_RESET}$ during $^{t}PW\_RESET$, otherwise the DRAM may not be reset.
4. Undershoot should not exceed the V_{IN} shown in the Absolute Maximum Ratings table.
5. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
6. RESET is destructive to data contents.
7. See RESET Procedure at Power Stable Condition figure.

Figure 211: RESET_n Input Slew Rate Definition



Command/Address Input Levels

Table 85: Command and Address Input Levels: DDR4-1600 Through DDR4-2400

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 100	$V_{DD}5$	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 75	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 75	mV	1, 2

Table 85: Command and Address Input Levels: DDR4-1600 Through DDR4-2400 (Continued)

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	$V_{IL(AC)}$	V_{SS}5	V_{REF} - 100	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	0.49 × V_{DD}	0.51 × V_{DD}	V	4

Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet ^{t}IS timings and $V_{IL}/V_{IH(DC)}$ to meet ^{t}IH timings.
4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% V_{DD} (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 86: Command and Address Input Levels: DDR4-2666

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 90	V_{DD}5	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 65	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	V_{SS}5	V_{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	0.49 × V_{DD}	0.51 × V_{DD}	V	4

Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet ^{t}IS timings and $V_{IL}/V_{IH(DC)}$ to meet ^{t}IH timings.
4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% V_{DD} (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 87: Command and Address Input Levels: DDR4-2933 and DDR4-3200

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 90	V_{DD}5	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 65	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	V_{SS}5	V_{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	0.49 × V_{DD}	0.51 × V_{DD}	V	4

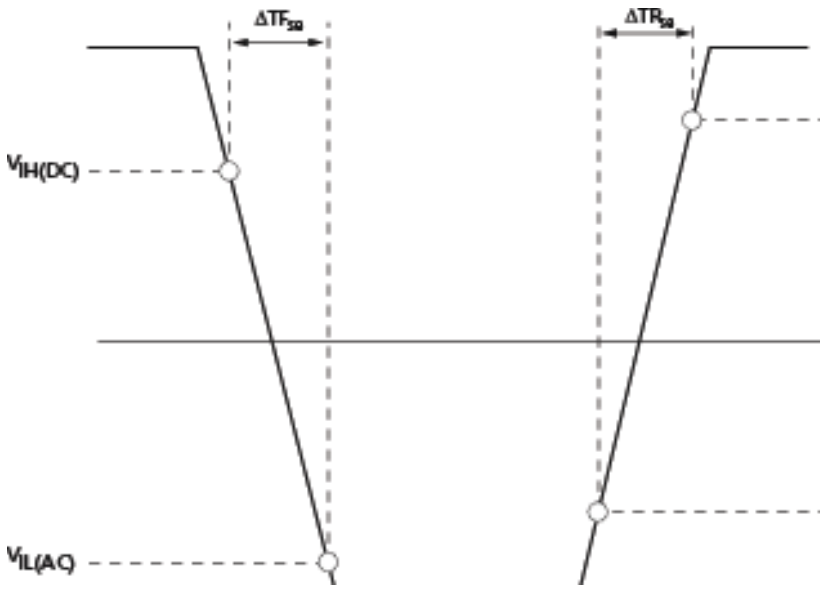
Notes: 1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet ^{t}IS timings and $V_{IL}/V_{IH(DC)}$ to meet ^{t}IH timings.
4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% V_{DD} (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 88: Single-Ended Input Slew Rates

Parameter	Symbol	Min	Max	Unit	Note
Single-ended input slew rate – CA	SR_{CA}	1.0	7.0	V/ns	1, 2, 3, 4

Notes: 1. For input except RESET_n.
2. $V_{REF} = V_{REFCA(DC)}$.
3. $^{t}IS/^{t}IH$ timings assume SR_{CA} = 1V/ns.
4. Measured between $V_{IH(AC)}$ and $V_{IL(AC)}$ for falling edges and between $V_{IL(AC)}$ and $V_{IH(AC)}$ for rising edges

Figure 212: Single-Ended Input Slew Rate Definition



Command, Control, and Address Setup, Hold, and Derating

The total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated to account for slew rate variation by adding the data sheet ^{t}IS (base) values, the $V_{IL(AC)}/V_{IH(AC)}$ points, and ^{t}IH (base) values, the $V_{IL(DC)}/V_{IH(DC)}$ points; to the $\Delta^{t}IS$ and $\Delta^{t}IH$ derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2 V/ns. Example: ^{t}IS (total setup time) = ^{t}IS (base) + $\Delta^{t}IS$. For a valid transition, the input signal has to remain above/below $V_{IH(AC)}/V_{IL(AC)}$ for the time defined by ^{t}VAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$. For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (^{t}IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{IH(AC)min}$ that does not ring back below $V_{IH(DC)min}$. Setup (^{t}IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{IL(AC)max}$ that does not ring back above $V_{IL(DC)max}$.

Hold (^{t}IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{IH(AC)min}$ that does not ring back below $V_{IH(DC)min}$. Hold (^{t}IH)

nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{IL(AC)min}$ that does not ring back above $V_{IL(DC)max}$.

Table 89: Command and Address Setup and Hold Values Referenced – AC/DC-Based

Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
^{t}IS(base, AC100)	115	100	80	62	–	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IH(base, DC75)	140	125	105	87	–	–	–	ps	$V_{IH(DC)}/V_{IL(DC)}$
^{t}IS(base, AC90)	–	–	–	–	55	48	40	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IH(base, DC65)	–	–	–	–	80	73	65	ps	$V_{IH(DC)}/V_{IL(DC)}$
$^{t}IS/^{t}IH$(Vref)	215	200	180	162	145	138	130	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 90: Derating Values for $^{t}IS/^{t}IH$ – AC100DC75-Based

$\Delta^{t}IS$ with AC100 Threshold, $\Delta^{t}IH$ with DC75 Threshold Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$	$\Delta^{t}IS$	$\Delta^{t}IH$
7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
1.0	–10	–10	–9	–9	–8	–8	–6	–6	–4	–4	**0**	**0**	8	8	25	25
0.9	–17	–14	–16	–14	–15	–13	–13	–10	–11	–8	–7	–4	1	4	18	21
0.8	–26	–19	–25	–19	–24	–18	–22	–16	–20	–14	–16	–9	–7	–1	9	16
0.7	–37	–26	–36	–25	–35	–24	–33	–22	–31	–20	–27	–16	–18	–8	–2	9
0.6	–52	–35	–51	–34	–50	–33	–48	–31	–46	–29	–42	–25	–33	–17	–17	0
0.5	–73	–48	–72	–47	–71	–46	–69	–44	–67	–42	–63	–38	–54	–29	–38	–13
0.4	–104	–66	–103	–66	–102	–65	–100	–63	–98	–60	–94	–56	–85	–48	–69	–31

Table 91: Derating Values for ^{t}IS/^{t}IH – AC90/DC65-Based

Δ^{t}IS with AC90 Threshold, Δ^{t}IH with DC65 Threshold Derating (ps) – AC/DC-Based																
CMD/ADD R Slew Rate V/ns	CK, CK# Differential Slew Rate															
	10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IH	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
1.0	–9	–9	–8	–8	–8	–8	–6	–6	–4	–4	**0**	**0**	8	8	23	23
0.9	–15	–13	–15	–12	–14	–11	–12	–9	–10	–7	–6	–4	1	4	16	19
0.8	–23	–17	–23	–17	–22	–16	–20	–14	–18	–12	–14	–8	–7	–1	8	14
0.7	–34	–23	–33	–22	–32	–21	–30	–20	–28	–18	–25	–14	–17	–6	–2	9
0.6	–47	–31	–47	–30	–46	–29	–44	–27	–42	–25	–38	–22	–31	–14	–16	1
0.5	–67	–42	–66	–41	–65	–40	–63	–38	–61	–36	–58	–33	–50	–25	–35	–10
0.4	–95	–58	–95	–57	–94	–56	–92	–54	–90	–53	–86	–49	–79	–41	–64	–26

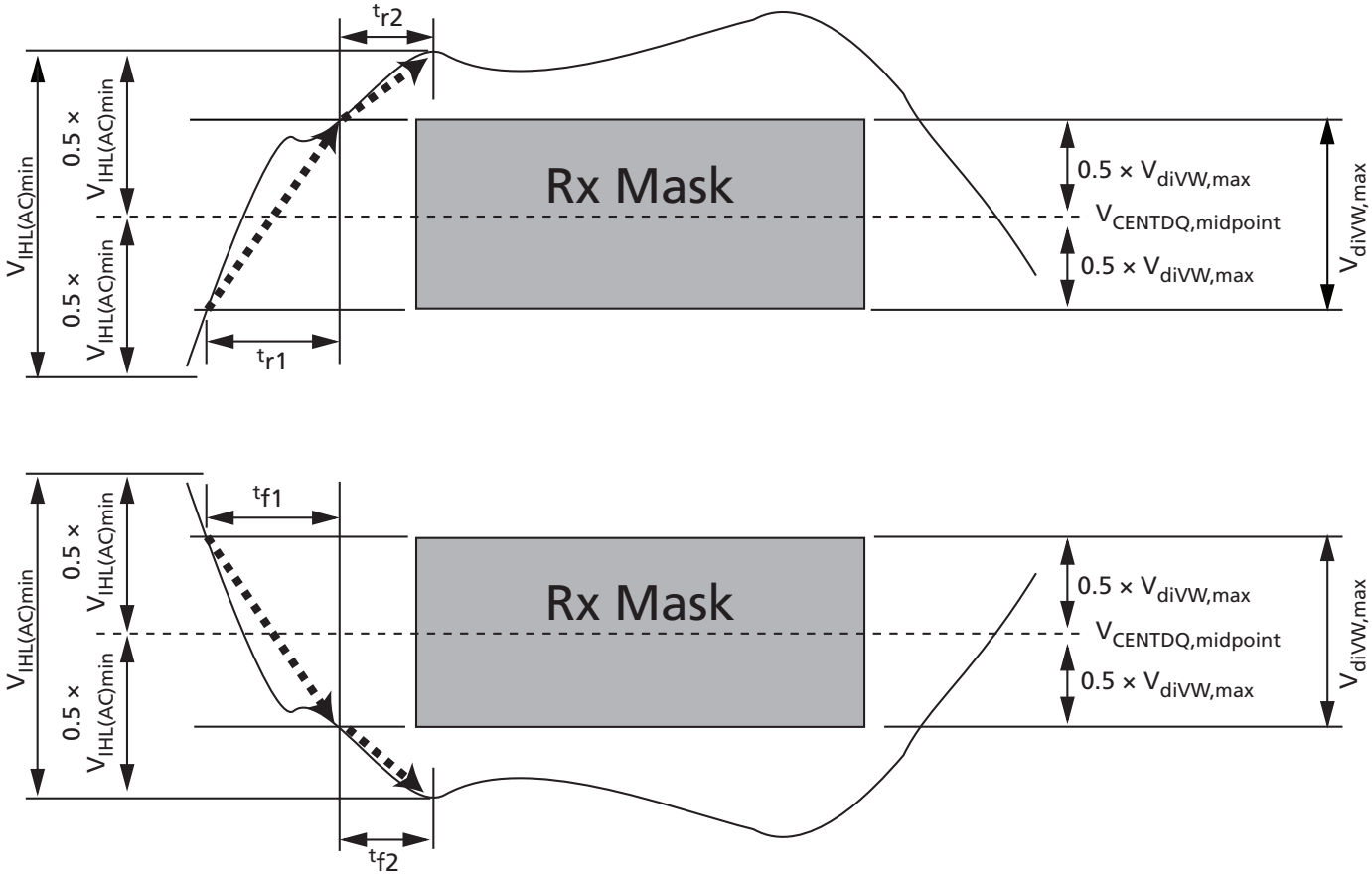
Data Receiver Input Requirements

The following parameters apply to the data receiver Rx MASK operation detailed in the Write Timing section, Data Strobe-to-Data Relationship.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in the figure below. A LOW-to-HIGH transition time, tr1, is measured from 0.5 × $V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the last transition through 0.5 × $V_{diVW,max}$ above $V_{CENTDQ,midpoint}$; tr2 is measured from the last transition through 0.5 × $V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the first transition through the 0.5 × $V_{IHL(AC)min}$ above $V_{CENTDQ,midpoint}$.

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in the figure below. A HIGH-to-LOW transition time, tf1, is measured from 0.5 × $V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the last transition through 0.5 × $V_{diVW,max}$ below $V_{CENTDQ,midpoint}$; tf2 is measured from the last transition through 0.5 × $V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the first transition through the 0.5 × $V_{IHL(AC)min}$ below $V_{CENTDQ,midpoint}$.

Figure 213: DQ Slew Rate Definitions



Notes: 1. Rising edge slew rate equation srr1 = $V_{diVW,max}/({}^{t}r1)$.
2. Rising edge slew rate equation srr2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 \times {}^{t}r2)$.
3. Falling edge slew rate equation srf1 = $V_{diVW,max}/({}^{t}f1)$.
4. Falling edge slew rate equation srf2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 \times {}^{t}f2)$.

Table 92: DQ Input Receiver Specifications

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V_{IN} Rx mask input peak-to-peak	V_{diVW}	–	136	–	130	–	120	–	115	–	110	mV	2, 3
DQ Rx input timing window	TdiVW	–	0.2	–	0.2	–	0.22	–	0.23	–	0.23	UI	2, 3
DQ AC input swing peak-to-peak	$V_{IHL(AC)}$	186	–	160	–	150	–	145	–	140	–	mV	4, 5
DQ input pulse width	TdiPW	0.58	–	0.58	–	0.58	–	0.58	–	0.58	–	UI	6

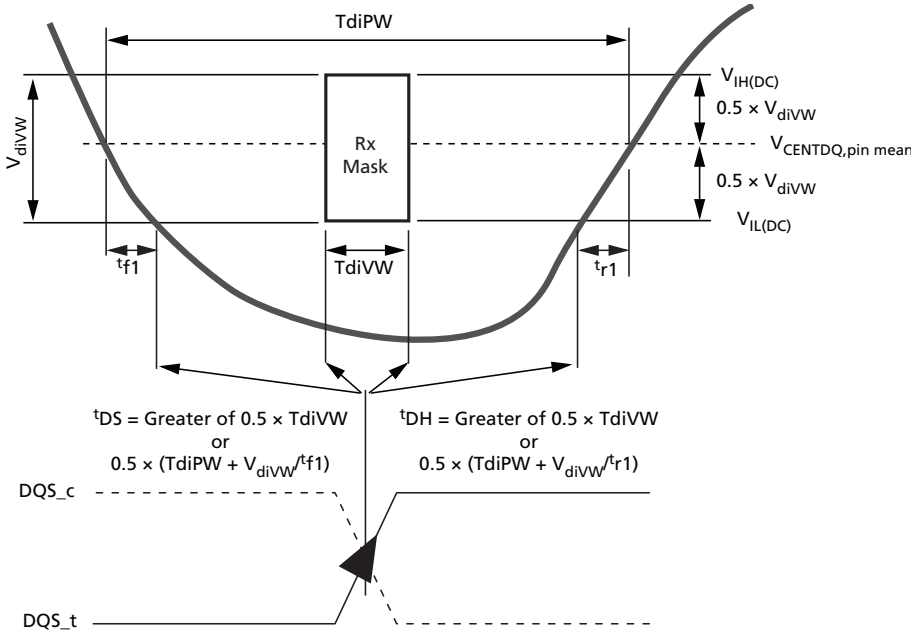
Table 92: DQ Input Receiver Specifications (Continued)

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS-to-DQ Rx mask offset	^{t}DQS2DQ	–0.17	0.17	–0.17	0.17	–0.19	0.19	–0.22	0.22	–0.22	0.22	UI	7
DQ-to-DQ Rx mask offset	^{t}DQ2DQ	–	0.1	–	0.1	–	0.105	–	0.115	–	0.125	UI	8
Input slew rate over V_{diVW} if ^{t}CK ≥ 0.937ns	srr1, srf1	1	9	1	9	1	9	1	9	1	9	V/ns	9
Input slew rate over V_{diVW} if 0.937ns > ^{t}CK ≥ 0.625ns	srr1, srf1	–	–	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	9
Rising input slew rate over 1/2 $V_{IHL(AC)}$	srr2	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	V/ns	10
Falling input slew rate over 1/2 $V_{IHL(AC)}$	srf2	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	V/ns	10

Notes:
1. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW (MIN), $V_{diVW,max}$, and minimum slew rate limits, then either TdiVW (MIN) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.
2. Data Rx mask voltage and timing total input valid window where V_{diVW} is centered around $V_{CENTDQ,midpoint}$ after V_{REFDQ} training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER =1^{e-16} when the Rx mask is not violated.
3. Defined over the DQ internal V_{REF} range 1.
4. Overshoot and undershoot specifications apply.
5. DQ input pulse signal swing into the receiver must meet or exceed $V_{IHL(AC)min}$. $V_{IHL(AC)min}$ is to be achieved on an UI basis when a rising and falling edge occur in the same UI (a valid TdiPW).
6. DQ minimum input pulse width defined at the $V_{CENTDQ,midpoint}$.
7. DQS-to-DQ Rx mask offset is skew between DQS and DQ within a nibble (x4) or word (x8, x16 [for x16, the upper and lower bytes are treated as separate x8s]) at the SDRAM balls over process, voltage, and temperature.
8. DQ-to-DQ Rx mask offset is skew between DQs within a nibble (x4) or word (x8, x16) at the SDRAM balls for a given component over process, voltage, and temperature.
9. Input slew rate over V_{diVW} mask centered at $V_{CENTDQ,midpoint}$. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
10. Input slew rate between V_{diVW} mask edge and $V_{IHL(AC)min}$ points.
11. Note 1 applies to the entire table.

The following figure shows the Rx mask relationship to the input timing specifications relative to system ^{t}DS and ^{t}DH. The classical definition for ^{t}DS/^{t}DH required a DQ rising and falling edges to not violate ^{t}DS and ^{t}DH relative to the DQS strobe at any time; however, with the Rx mask ^{t}DS and ^{t}DH can shift relative to the DQS strobe provided the input pulse width specification is satisfied and the Rx mask is not violated.

Figure 214: Rx Mask Relative to ^{t}DS/^{t}DH



The following figure and table show an example of the worst case Rx mask required if the DQS and DQ pins do not have DRAM controller to DRAM write DQ training. The figure and table show that without DRAM write DQ training, the Rx mask would increase from 0.2UI to essentially 0.54UI. This would also be the minimum ^{t}DS and ^{t}DH required as well.

Figure 215: Rx Mask Without Write Training

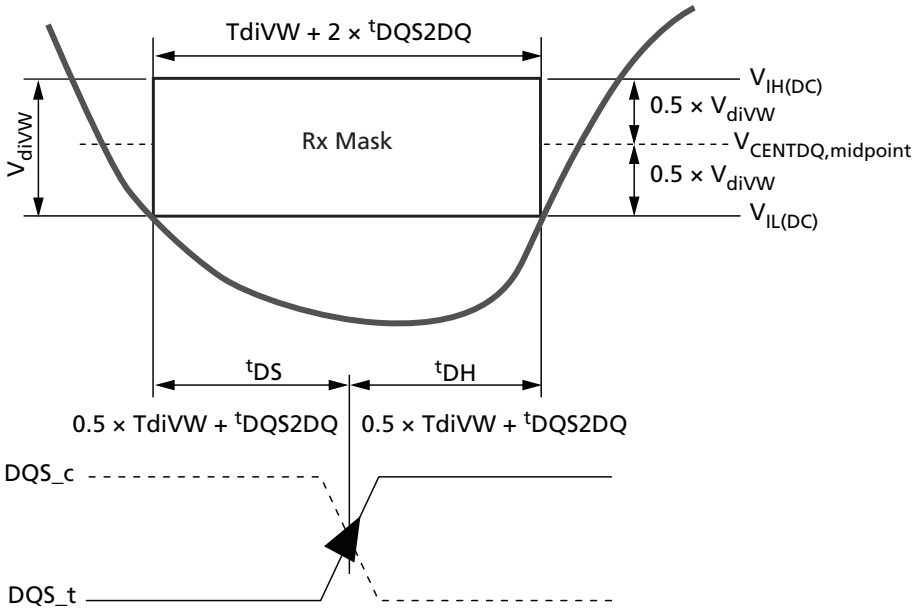


Table 93: Rx Mask and ^{t}DS/^{t}DH without Write Training

DDR4	$V_{IHL(AC)}$ (mV)	TdiPW (UI)	V_{diVW} (mV)	TdiVW (UI)	^{t}DQS2DQ (UI)	^{t}DQ2DQ (UI)	Rx Mask with Write Train (ps)	^{t}DS + ^{t}DH (ps)
1600	186	0.58	136	0.2	±0.17	0.1	125	338
1866	186	0.58	136	0.2	±0.17	0.1	107.1	289
2133	186	0.58	136	0.2	±0.17	0.1	94	253
2400	160	0.58	130	0.2	±0.17	0.1	83.3	225
2666	150	0.58	120	0.22	±0.19	0.105	82.5	225
2933	145	0.58	115	0.23	±0.22	0.115	78.4	228
3200	140	0.58	110	0.23	±0.22	0.125	71.8	209

Notes: 1. $V_{IHL(AC)}$, V_{diVW}, and $V_{ILH(DC)}$ referenced to $V_{CENTDQ,midpoint}$.

Connectivity Test (CT) Mode Input Levels

Table 94: TEN Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
TEN AC input high voltage	$V_{IH(AC)\_TEN}$	0.8 × V_{DD}	V_{DD}	V	1
TEN DC input high voltage	$V_{IH(DC)\_TEN}$	0.7 × V_{DD}	V_{DD}	V	
TEN DC input low voltage	$V_{IL(DC)\_TEN}$	V_{SS}	0.3 × V_{DD}	V	
TEN AC input low voltage	$V_{IL(AC)\_TEN}$	V_{SS}	0.2 × V_{DD}	V	2
TEN falling time	$^{t}F\_TEN$	–	1 0	ns	

Table 94: TEN Input Levels (CMOS) (Continued)

Parameter	Symbol	Min	Max	Unit	Note
TEN rising time	$^{t}R\_TEN$	–	1 0	ns	

Notes: 1. Overshoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
2. Undershoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.

Figure 216: TEN Input Slew Rate Definition

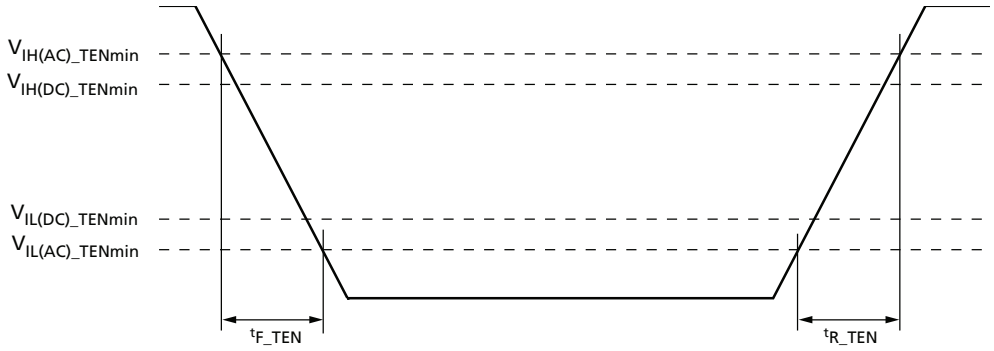


Table 95: CT Type-A Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipA AC input high voltage	$V_{IH(AC)}$	V_{REF} + 200	V_{DD1}[1]	V	2, 3
CTipA DC input high voltage	$V_{IH(DC)}$	V_{REF} + 150	V_{DD}	V	2, 3
CTipA DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 150	V	2, 3
CTipA AC input low voltage	$V_{IL(AC)}$	V_{SS1}[1]	V_{REF} - 200	V	2, 3
CTipA falling time	$^{t}F\_CTipA$	–	5	ns	2
CTipA rising time	$^{t}R\_CTipA$	–	5	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-A inputs: CS_n, BG[1:0], BA[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, A17, CKE, ACT_n, ODT, CLK_t, CLK_C, PAR.
3. $V_{REFCA} = 0.5 \times V_{DD}$.

Figure 217: CT Type-A Input Slew Rate Definition

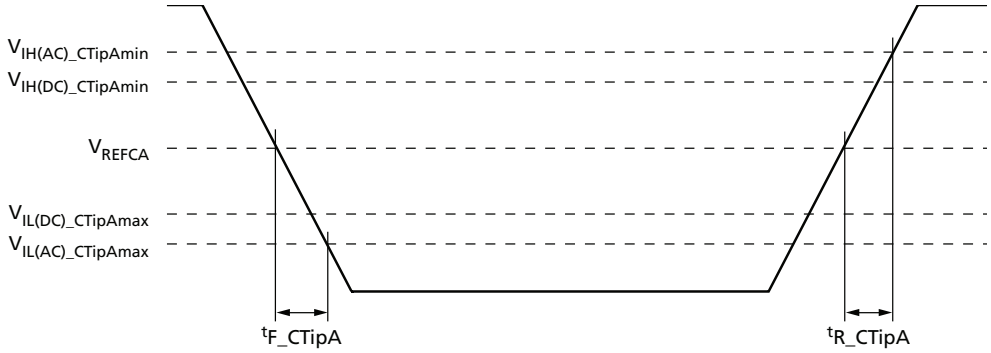


Table 96: CT Type-B Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipB AC input high voltage	$V_{IH(AC)}$	V_{REF} + 300	V_{DD1} [1]	V	2, 3
CTipB DC input high voltage	$V_{IH(DC)}$	V_{REF} + 200	V_{DD}	V	2, 3
CTipB DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 200	V	2, 3
CTipB AC input low voltage	$V_{IL(AC)}$	V_{SS1} [1]	V_{REF} - 300	V	2, 3
CTipB falling time	$^{t}F_{CTipB}$	–	5	ns	2
CTipB rising time	$^{t}R_{CTipB}$	–	5	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-B inputs: DML_n/DBIL_n, DMU_n/DBIU_n and DM_n/DBI_n.
3. V_{REFDQ} should be 0.5 × V_{DD}

Figure 218: CT Type-B Input Slew Rate Definition

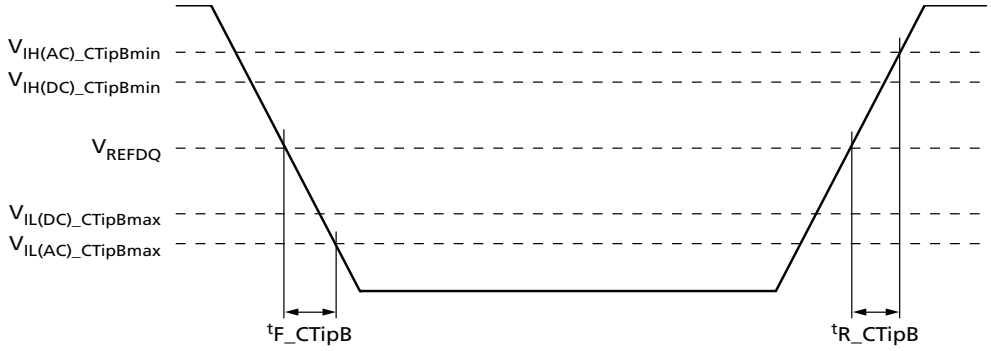


Table 97: CT Type-C Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
CTipC AC input high voltage	$V_{IH(AC)\_CTipC}$	0.8 × V_{DD}	V_{DD} [1]	V	2
CTipC DC input high voltage	$V_{IH(DC)\_CTipC}$	0.7 × V_{DD}	V_{DD}	V	2
CTipC DC input low voltage	$V_{IL(DC)\_CTipC}$	V_{SS}	0.3 × V_{DD}	V	2
CTipC AC input low voltage	$V_{IL(AC)\_CTipC}$	V_{SS} [1]	0.2 × V_{DD}	V	2

Table 97: CT Type-C Input Levels (CMOS) (Continued)

Parameter	Symbol	Min	Max	Unit	Note
CTipC falling time	$^{t}F\_CTipC$	–	1 0	ns	2
CTipC rising time	$^{t}R\_CTipC$	–	1 0	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-C inputs: Alert_n.

Figure 219: CT Type-C Input Slew Rate Definition

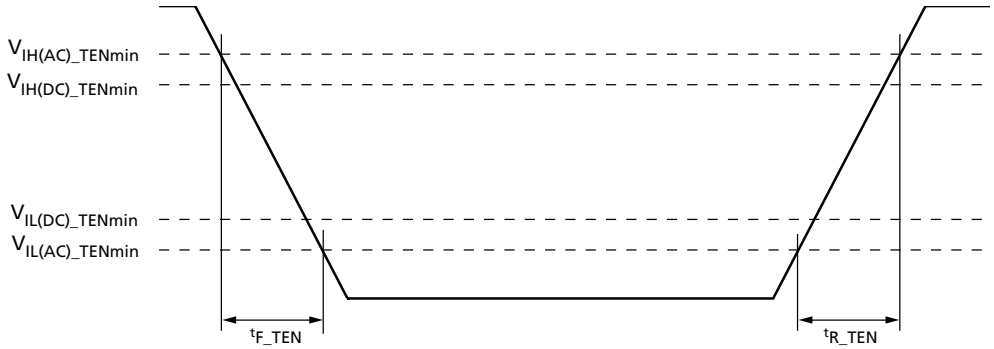
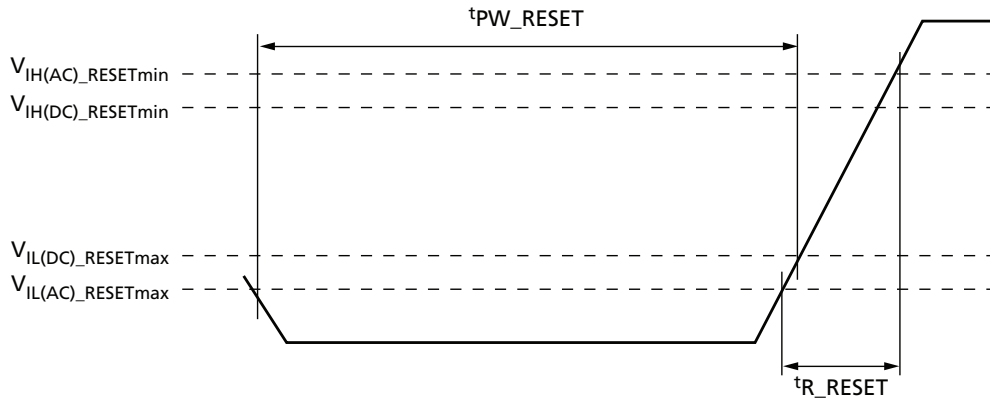


Table 98: CT Type-D Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipD AC input high voltage	$V_{IH(AC)\_CTipD}$	0.8 × V_{DD}	V_{DD}	V	4
CTipD DC input high voltage	$V_{IH(DC)\_CTipD}$	0.7 × V_{DD}	V_{DD}	V	2
CTipD DC input low voltage	$V_{IL(DC)\_CTipD}$	V_{SS}	0.3 × V_{DD}	V	1
CTipD AC input low voltage	$V_{IL(AC)\_CTipD}$	V_{SS}	0.2 × V_{DD}	V	5
Rising time	$^{t}R\_RESET$	–	1	µs	3
RESET pulse width - after power-up	$^{t}PW\_RESET\_S$	1	–	µs	
RESET pulse width - during power-up	$^{t}PW\_RESET\_L$	200	–	µs	

Notes: 1. After RESET_n is registered LOW, the RESET_n level must be maintained below $V_{IL(DC)\_RESET}$ during $^{t}PW\_RESET$, otherwise, the DRAM may not be reset.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above $V_{IH(DC)\_RESET}$, otherwise, operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
4. Overshoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
5. Undershoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
6. CT Type-D inputs: RESET_n; same requirements as in normal mode.

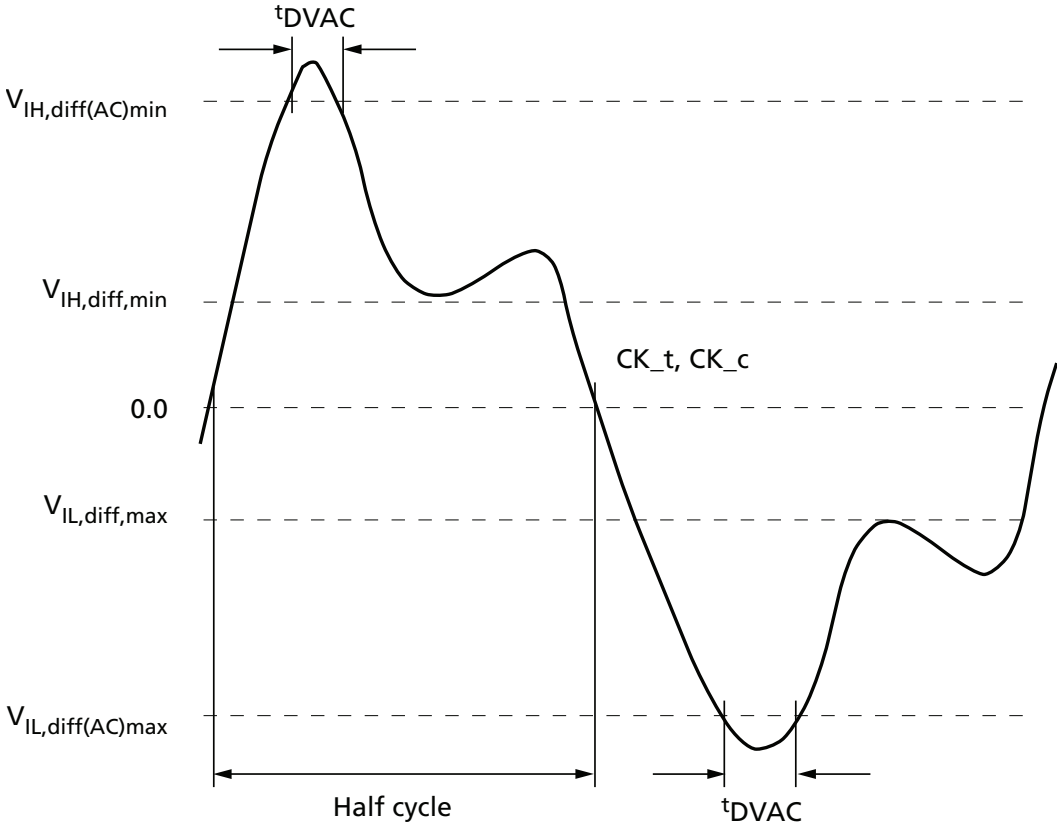
Figure 220: CT Type-D Input Slew Rate Definition



Electrical Characteristics – AC and DC Differential Input Measurement Levels

Differential Inputs

Figure 221: Differential AC Swing and "Time Exceeding AC-Level" tDVAC



Notes: 1. Differential signal rising edge from $V_{IL,diff,max}$ to $V_{IH,diff(AC)min}$ must be monotonic slope.

2. Differential signal falling edge from $_{IH,diff,min}$ to $V_{IL,diff(AC)max}$ must be monotonic slope.

Table 99: Differential Input Swing Requirements for CK_t, CK_c

Parameter	Symbol	DDR4-1600 / 1866 / 2133		DDR4-2400 / 2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Differential input high	V_{IHdiff}	150	Note 3	135	Note 3	125	Note 3	110	Note 3	mV	1
Differential input low	V_{ILdiff}	Note 3	–150	Note 3	-135	Note 3	-125	Note 3	-110	mV	1
Differential input high (AC)	$V_{IH-diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	Note 3	2 × ($V_{IH(AC)}$ - V_{REF})	Note 3	2 × ($V_{IH(AC)}$ - V_{REF})	Note 3	2 × ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2
Differential input low (AC)	$V_{IL-diff(AC)}$	Note 3	2 × ($V_{IL(AC)}$ - V_{REF})	Note 3	2 × ($V_{IL(AC)}$ - V_{REF})	Note 3	2 × ($V_{IL(AC)}$ - V_{REF})	Note 3	2 × ($V_{IL(AC)}$ - V_{REF})	V	2

Notes: 1. Used to define a differential signal slew-rate.
2. For CK_t, CK_c use $V_{IH(AC)}$ and $V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
3. These values are not defined; however, the differential signals (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

Table 100: Minimum Time AC Time ^{t}DVAC for CK

Slew Rate (V/ns)	^{t}DVAC (ps) at $\lvert V_{IH,diff(AC)}$ to $V_{IL,diff(AC)}\rvert$	
	200mV	TBDmV
>4.0	120	TBD
4.0	115	TBD
3.0	110	TBD
2.0	105	TBD
1.9	100	TBD
1.6	95	TBD
1.4	90	TBD
1.2	85	TBD
1.0	80	TBD
<1.0	80	TBD

Notes: 1. Below $V_{IL(AC)}$.

Single-Ended Requirements for CK Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has to comply with certain requirements for single-ended signals. CK_t and CK_c have to reach approximately $V_{SEHmin}/V_{SEL,max}$, which are approximately equal to the AC levels $V_{IH(AC)}$ and $V_{IL(AC)}$ for ADD/CMD signals in every half-cycle. The applicable AC levels for ADD/CMD might differ per speed-bin, and so on. For example, if a value other than 100mV is used for ADD/CMD $V_{IH(AC)}$ and $V_{IL(AC)}$ signals, then these AC levels also apply for the single-ended signals CK_t and CK_c.

While ADD/CMD signal requirements are with respect to V_{REFCA}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL,max}/V_{SEH,min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Figure 222: Single-Ended Requirements for CK

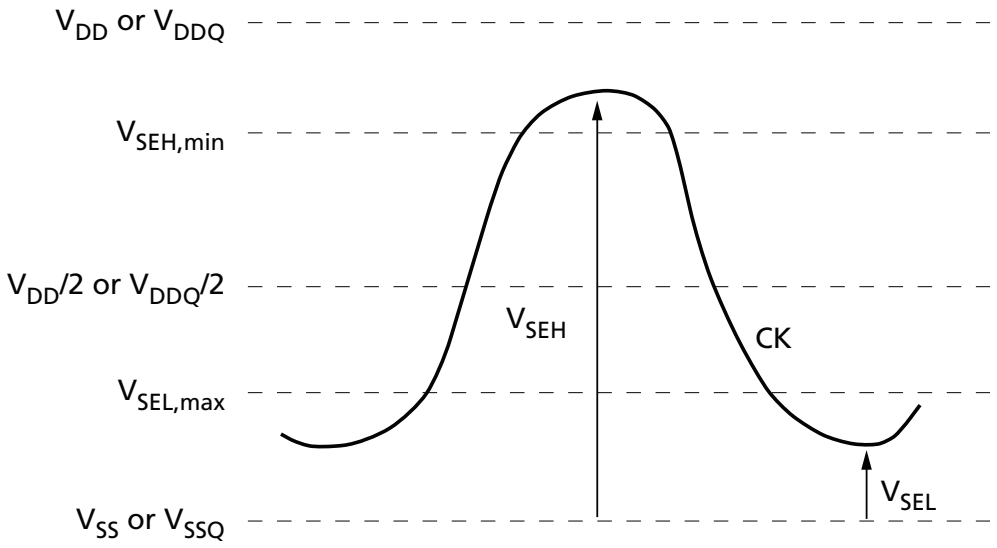


Table 101: Single-Ended Requirements for CK

Parameter	Symbol	DDR4-1600 / 1866 / 2133		DDR4-2400 / 2666		DDR4-2933 / 3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Single-ended high level for CK_t, CK_c	V_{SEH}	$V_{DD}/2$ + 0.100	Note 3	$V_{DD}/2$ + 0.095	Note 3	$V_{DD}/2$ + 0.085	Note 3	V	1, 2
Single-ended low level for CK_t, CK_c	V_{SEL}	Note 3	$V_{DD}/2$ - 0.100	Note 3	$V_{DD}/2$ - 0.095	Note 3	$V_{DD}/2$ - 0.085	V	1, 2

Notes: 1. For CK_t, CK_c use $V_{IH(AC)}$ and $V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
2. ADDR/CMD $V_{IH(AC)}$ and $V_{IL(AC)}$ based on V_{REFCA}.
3. These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

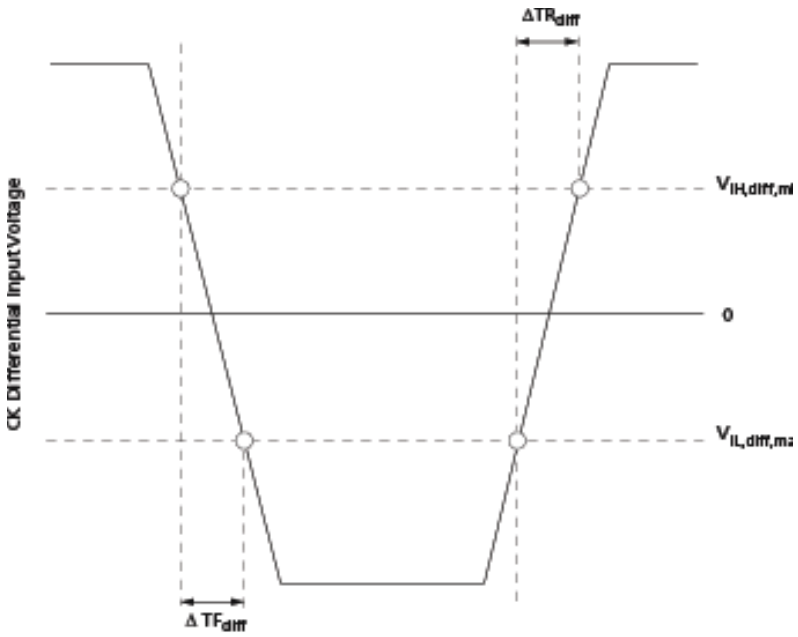
Slew Rate Definitions for CK Differential Input Signals

Table 102: CK Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$\lvert V_{IH,diff,min} - V_{IL,diff,max}\rvert / \Delta TR_{diff}$
Differential input slew rate for falling edge	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$\lvert V_{IH,diff,min} - V_{IL,diff,max}\rvert / \Delta TF_{diff}$

Notes: 1. The differential signal CK_t, CK_c must be monotonic between these thresholds.

Figure 223: Differential Input Slew Rate Definition for CK_t, CK_c



CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK_t, CK_c must meet the requirements shown below. The differential input cross point voltage $V_{IX(CK)}$ is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

Figure 224: $V_{IX(CK)}$ Definition

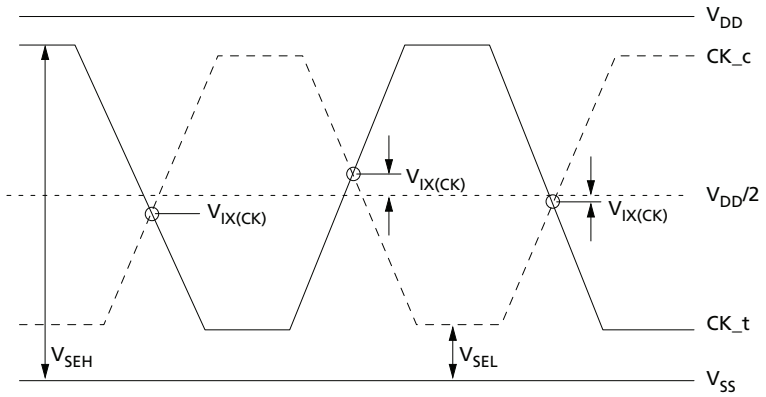


Table 103: Cross Point Voltage For CK Differential Input Signals at DDR4-1600 through DDR4-2400

Parameter	Sym	Input Level	DDR4-1600, 1866, 2133, 2400	
			Min	Max
Differential input cross point voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{IX(CK)}$	$V_{SEH} > V_{DD}/2 + 145mV$	N/A	120mV
		$V_{DD}/2 + 100mV \le V_{SEH} \le V_{DD}/2 + 145mV$	N/A	$(V_{SEH} - V_{DD}/2) - 25mV$
		$V_{DD}/2 - 145mV \le V_{SEL} \le V_{DD}/2 - 100mV$	$-(V_{DD}/2 - V_{SEL}) + 25mV$	N/A
		$V_{SEL} < V_{DD}/2 - 145mV$	–120mV	N/A

Table 104: Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200

Parameter	Sym	Input Level	DDR4-2666, 2933, 3200	
			Min	Max
Differential input cross point voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{IX(CK)}$	$V_{SEH} > V_{DD}/2 + 145mV$	N/A	110mV
		$V_{DD}/2 + 90mV \le V_{SEH} \le V_{DD}/2 + 145mV$	N/A	$(V_{SEH} - V_{DD}/2) - 30mV$
		$V_{DD}/2 - 145mV \le V_{SEL} \le V_{DD}/2 - 90mV$	$-(V_{DD}/2 - V_{SEL}) + 30mV$	N/A
		$V_{SEL} < V_{DD}/2 - 145mV$	–110mV	N/A

DQS Differential Input Signal Definition and Swing Requirements

Figure 225: Differential Input Signal Definition for DQS_t, DQS_c

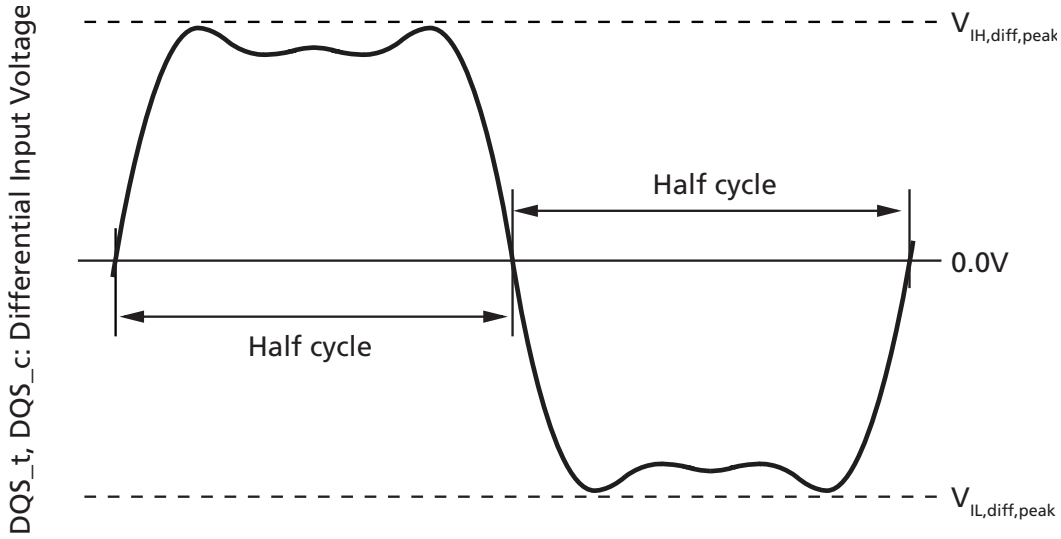


Table 105: DDR4-1600 through DDR4-2400 Differential Input Swing Requirements for DQS_t, DQS_c

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	186	V_{DDQ}	160	V_{DDQ}	mV	1, 2
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–186	V_{SSQ}	–160	mV	1, 2

Notes: 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

Table 106: DDR4-2633 through DDR4-3200 Differential Input Swing Requirements for DQS_t, DQS_c

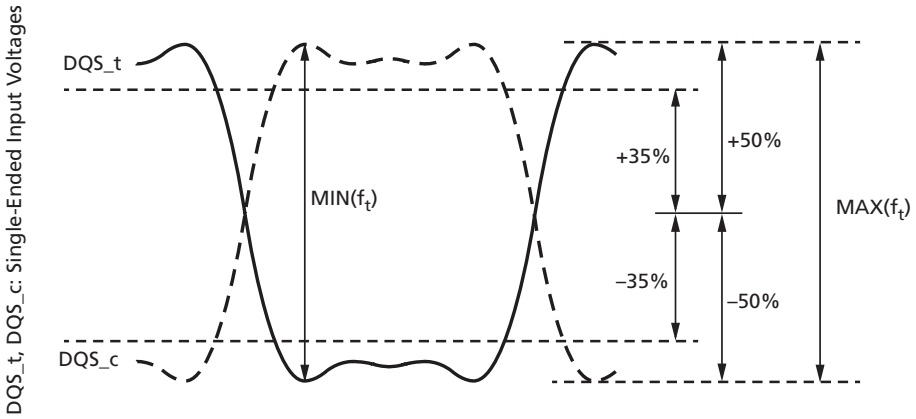
Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	150	V_{DDQ}	145	V_{DDQ}	140	V_{DDQ}	mV	1, 2
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–150	V_{SSQ}	–145	V_{SSQ}	–140	mV	1, 2

Notes: 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

The peak voltage of the DQS signals are calculated using the following equations: $V_{IH,dif,Peak}$ voltage = MAX(f_t)
$V_{IL,dif,Peak}$ voltage = MIN(f_t)
(f_t) = DQS_t, DQS_c.

The MAX(f(t)) or MIN(f(t)) used to determine the midpoint from which to reference the ±35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.

Figure 226: DQS_t, DQS_c Input Peak Voltage Calculation and Range of Exempt non-Monotonic Signaling



DQS Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet $V_{IX\_DQS,ratio}$ in the table below. The differential input cross point voltage V_{IX_DQS} ($V_{IX\_DQS\_FR}$ and $V_{IX\_DQS\_RF}$) is measured from the actual cross point of DQS_t, DQS_c relative to the $V_{DQS,mid}$ of the DQS_t and DQS_c signals.

$V_{DQS,mid}$ is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above $V_{DQS,mid}$ of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals. A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within ±35% of the midpoint of either $V_{IH.DIFF.Peak}$ voltage (DQS_t rising) or $V_{IL.DIFF.Peak}$ voltage (DQS_c rising), as shown in the figure below.

A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in the figure below), and a ring-back's horizontal tangent is derived from its positive slope to zero slope transition (point B in the figure below) and is not a valid horizontal tangent; a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in the figure below), and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in the figure below) and is not a valid horizontal tangent.

Figure 227: V_{IXDQS} Definition

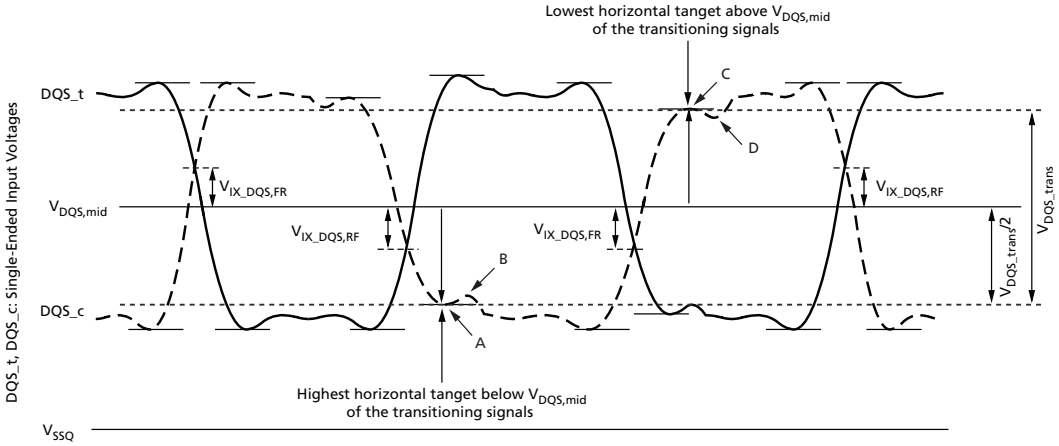


Table 107: Cross Point Voltage For Differential Input Signals DQS

Parameter	Symbol	DDR4-1600, 1866, 2133, 2400, 2666, 2933, 3200		Unit	Notes
		Min	Max		
DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	$V_{IX\_DQS,ratio}$	–	25	%	1, 2
$V_{DQS,mid}$ to $V_{cent(midpoint)}$ offset	$V_{DQS,mid\_to\_V\text{-}cent}$	–	Note 3	mV	2

Notes: 1. $V_{IX\_DQS,ratio}$ is DQS V_{IX} crossing ($V_{IX\_DQS,FR}$ or $V_{IX\_DQS,RF}$) divided by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above $V_{DQS,mid}$d of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals.
2. $V_{DQS,mid}$ will be similar to the V_{REFDQ} internal setting value ($V_{cent(midpoint)}$ offset) obtained during V_{REF} Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of $V_{IH,diff,DQS}$ minimum limit or 50mV.

Slew Rate Definitions for DQS Differential Input Signals

Table 108: DQS Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge	$V_{IL,diff,DQS}$	$V_{IH,diff,DQS}$	$\lvert V_{IH,diff,DQS} - V_{IL,diff,DQS}\rvert / \Delta TR_{diff}$
Differential input slew rate for falling edge	$V_{IH,diff,DQS}$	$V_{IL,diff,DQS}$	$\lvert V_{IHdiffDQS} - V_{IL,diff,DQS}\rvert / \Delta TF_{diff}$

Notes: 1. The differential signal DQS_t, DQS_c must be monotonic between these thresholds.

Figure 228: Differential Input Slew Rate and Input Level Definition for DQS_t, DQS_c

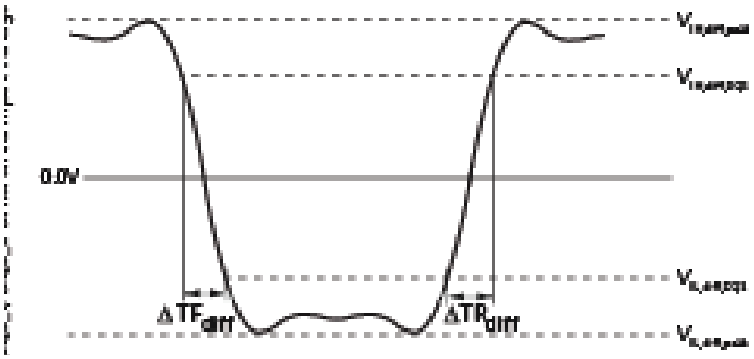


Table 109: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	186	V_{DDQ}	160	V_{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	136	–	130	–	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	–	–136	–	–130	mV	2, 3
Peak differential input low voltage	$V_{IL,diff,peak}$	$-V_{DDQ}$	–186	$-V_{DDQ}$	–160	mV	1
DQS differential input slew rate	SRIdiff	3.0	18	3.0	18	V/ns	4, 5

Notes: 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
4. Differential input slew rate for rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by $\lvert V_{IL,diff,min} - V_{IH,diff,max}\rvert / \Delta TR_{diff}$.

5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|/\Delta TF_{diff}$.

Table 110: DDR4-2666 through DDR4-3200 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	150	V_{DDQ}	145	V_{DDQ}	140	V_{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	130	–	115	–	110	–	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	–	–130	–	–115	–	–110	mV	2, 3
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–150	V_{SSQ}	–145	V_{SSQ}	–140	mV	1
DQS differential input slew rate	SRIdiff	2.5	18	2.5	18	2.5	18	V/ns	4, 5

Notes: 1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
4. Differential input slew rate for rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|/\Delta TR_{diff}$.
5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|/\Delta TF_{diff}$.

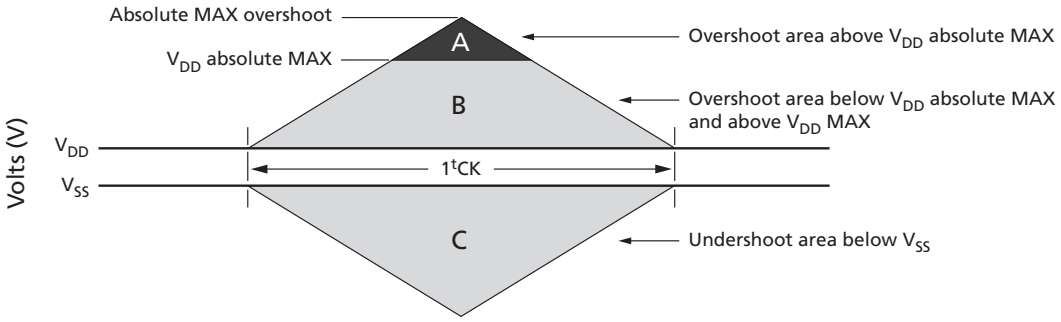
Electrical Characteristics – Overshoot and Undershoot Specifications

Address, Command, and Control Overshoot and Undershoot Specifications

Table 111: ADDR, CMD, CNTL Overshoot and Undershoot/Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Address and control pins (A[17:0], BG[1:0], BA[1:0], CS_n, RAS_n, CAS_n, WE_n, CKE, ODT, C2-0)								
Area A: Maximum peak amplitude above V_{DD} absolute MAX	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SS}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Area A maximum overshoot area per 1^tCK	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V/ns
Area B maximum overshoot area per 1^tCK	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V/ns
Area C maximum undershoot area per 1^tCK	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V/ns

Figure 229: ADDR, CMD, CNTL Overshoot and Undershoot Definition

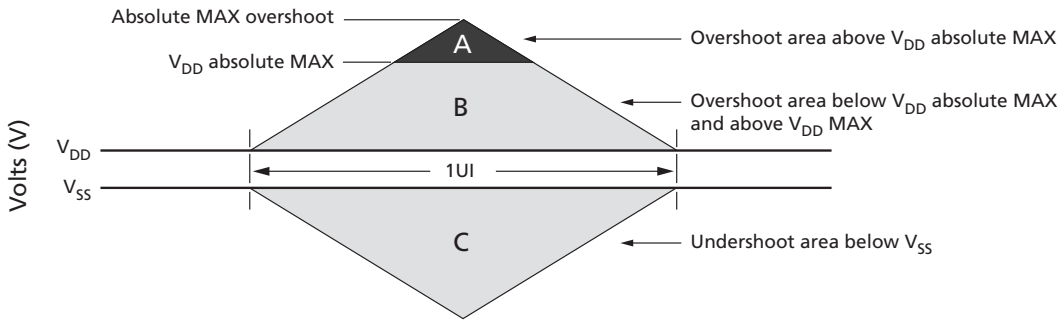


Clock Overshoot and Undershoot Specifications

Table 112: CK Overshoot and Undershoot/ Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
CLK_t, CLK_n								
Area A: Maximum peak amplitude above V_{DD} absolute MAX	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SS}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Area A maximum overshoot area per 1UI	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V/ns
Area B maximum overshoot area per 1UI	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V/ns
Area C maximum undershoot area per 1UI	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	0.0762	V/ns

Figure 230: CK Overshoot and Undershoot Definition

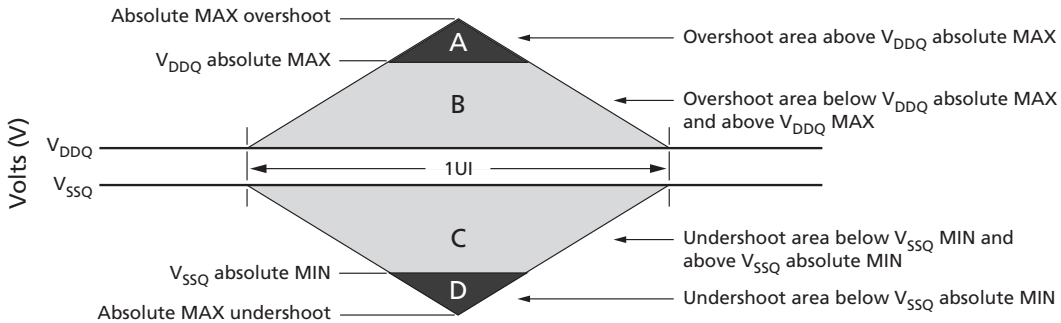


Data, Strobe, and Mask Overshoot and Undershoot Specifications

Table 113: Data, Strobe, and Mask Overshoot and Undershoot/ Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
DQS_t, DQS_n, LDQS_t, LDQS_n, UDQS_t, UDQS_n, DQ[0:15], DM/DBI, UDM/UDBI, LDM/LDBI,								
Area A: Maximum peak amplitude above V_{DDQ} absolute MAX	0.16	0.16	0.16	0.16	0.16	0.16	0.16	V
Area B: Amplitude allowed between V_{DDQ} and V_{DDQ} absolute MAX	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SSQ}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	V
Area D: Maximum peak amplitude below V_{SSQ} absolute MIN	0.10	0.10	0.10	0.10	0.10	0.10	0.10	V
Area A maximum overshoot area per 1UI	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V/ns
Area B maximum overshoot area per 1UI	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V/ns
Area C maximum undershoot area per 1UI	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V/ns
Area D maximum undershoot area per 1UI	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V/ns

Figure 231: Data, Strobe, and Mask Overshoot and Undershoot Definition



Electrical Characteristics – AC and DC Output Measurement Levels

Single-Ended Outputs

Table 114: Single-Ended Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	1.1 × V_{DDQ}	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	0.8 × V_{DDQ}	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	0.5 × V_{DDQ}	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	(0.7 + 0.15) × V_{DDQ}	V
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	(0.7 - 0.15) × V_{DDQ}	V

Notes: 1. The swing of ±0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 115: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TR_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TF_{se}$

Figure 232: Single-ended Output Slew Rate Definition

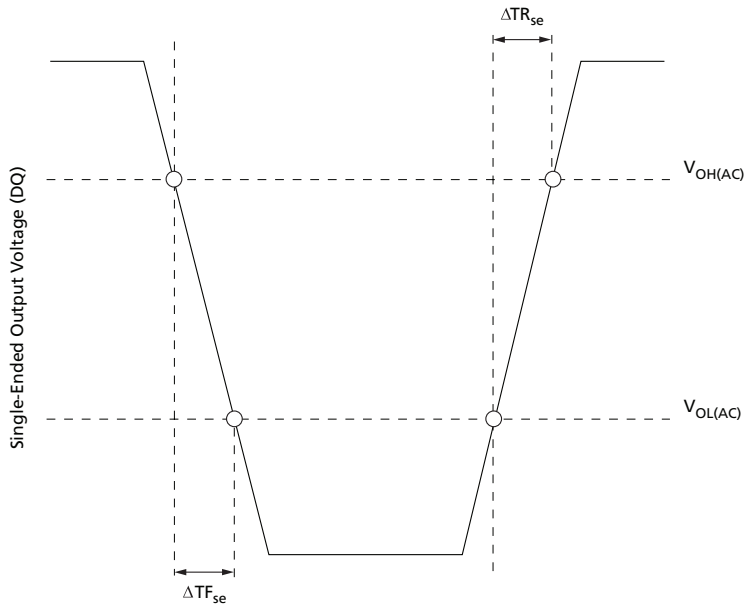


Table 116: Single-Ended Output Slew Rate

Parameter	Symbol	DDR4-1600/ 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Single-ended output slew rate	SRQ_{se}	4	9	4	9	4	9	V/ns

Notes: 1. SR = slew rate; Q = query output; se = single-ended signals.
2. In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane:
   - Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are static (they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from LOW-to-HIGH or HIGH-to-LOW, respectively). For the remaining DQ signal switching into the opposite direction, the standard maximum limit of 9 V/ns applies.
3. For $R_{ON} = R_{ZQ}/7$.

Differential Outputs

Table 117: Differential Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC differential output high measurement level (for output slew rate)	$V_{OH,diff(AC)}$	$0.3 \times V_{DDQ}$	V
AC differential output low measurement level (for output slew rate)	$V_{OL,diff(AC)}$	$-0.3 \times V_{DDQ}$	V

Notes: 1. The swing of ±0.3 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 118: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TF_{diff}$

Figure 233: Differential Output Slew Rate Definition

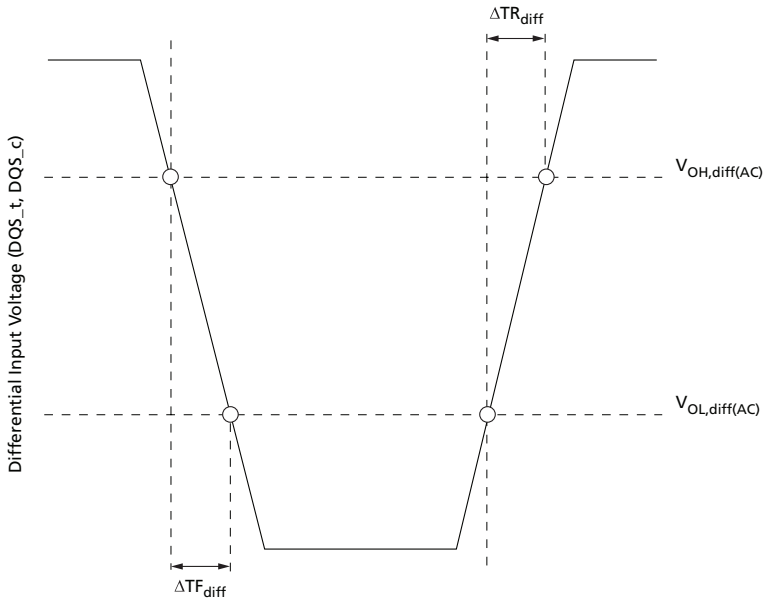


Table 119: Differential Output Slew Rate

Parameter	Symbol	DDR4-1600 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQ_{diff}	8	18	8	18	8	18	V/ns

Notes: 1. SR = slew rate; Q = query output; diff = differential signals.
2. For $R_{ON} = R_{ZQ}/7$.

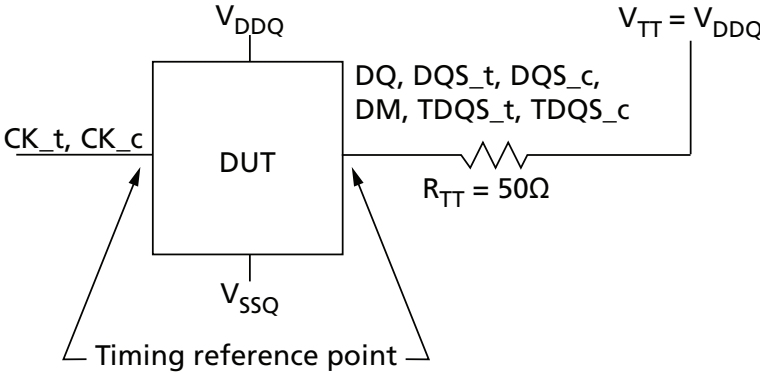
Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to $V_{TT} = V_{DDQ}$ and driver impedance of $R_{ZQ}/7$ for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device. The maximum DC high level of output signal = $1.0 \times V_{DDQ}$, the minimum DC low level of output signal = $\{ 34 / (34 + 50) \} \times V_{DDQ} = 0.4 \times V_{DDQ}$.

The nominal reference level of an output signal can be approximated by the following: The center of maximum DC high and minimum DC low = $\{ (1 + 0.4) / 2 \} \times V_{DDQ} = 0.7 \times V_{DDQ}$. The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 234: Reference Load For AC Timing and Output Slew Rate



Connectivity Test Mode Output Levels

Table 120: Connectivity Test Mode Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	$1.1 \times V_{DDQ}$	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	$0.5 \times V_{DDQ}$	V
DC output below measurement level (for IV curve linearity)	$V_{OB(DC)}$	$0.2 \times V_{DDQ}$	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	$V_{TT} + (0.1 \times V_{DDQ})$	V

Table 120: Connectivity Test Mode Output Levels (Continued)

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	V_{TT} - (0.1 × V_{DDQ})	V

Notes: 1. Driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Figure 235: Connectivity Test Mode Reference Test Load

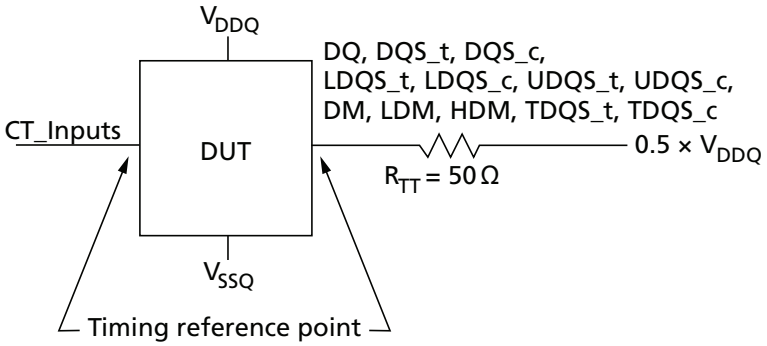


Figure 236: Connectivity Test Mode Output Slew Rate Definition

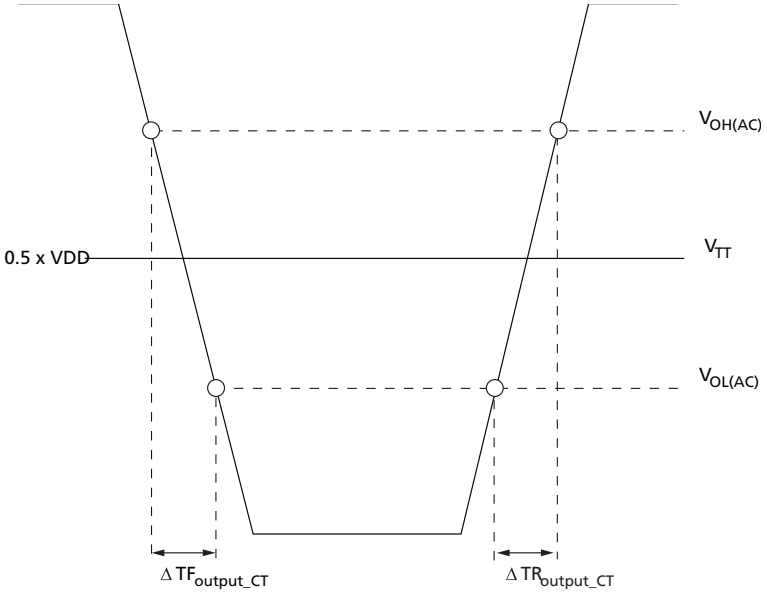


Table 121: Connectivity Test Mode Output Slew Rate

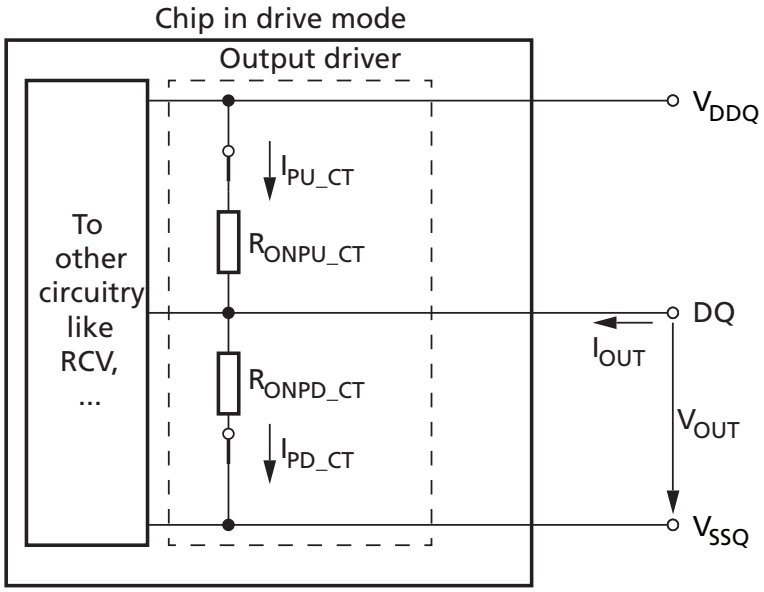
Parameter	Symbol	DDR4-1600 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Output signal falling time	TF_output_CT	–	10	–	10	–	10	ns/V
Output signal rising time	TR_output_CT	–	10	–	10	–	10	ns/V

Electrical Characteristics – AC and DC Output Driver Characteristics

Connectivity Test Mode Output Driver Electrical Characteristics

The DDR4 driver supports special values during connectivity test mode. These R_{ON} values are referenced in this section. A functional representation of the output buffer is shown in the figure below.

Figure 237: Output Driver During Connectivity Test Mode



The output driver impedance, R_{ON}, is determined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON} = R_{ZQ}/7$. This targets 34Ω with nominal $R_{ZQ} = 240Ω$; however, connectivity test mode uses uncalibrated drivers and only a maximum target is defined. Mismatch between pull up and pull down is undefined.

The individual pull-up and pull-down resistors (R_{ONPu_CT} and R_{ONPd_CT}) are defined as follows:

R_{ONPu_CT} when R_{ONPd_CT} is off:

$$R_{ONPU\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

R_{ONPD_CT} when R_{ONPU_CT} is off:

$$R_{ONPD\_CT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Table 122: Output Driver Electrical Characteristics During Connectivity Test Mode

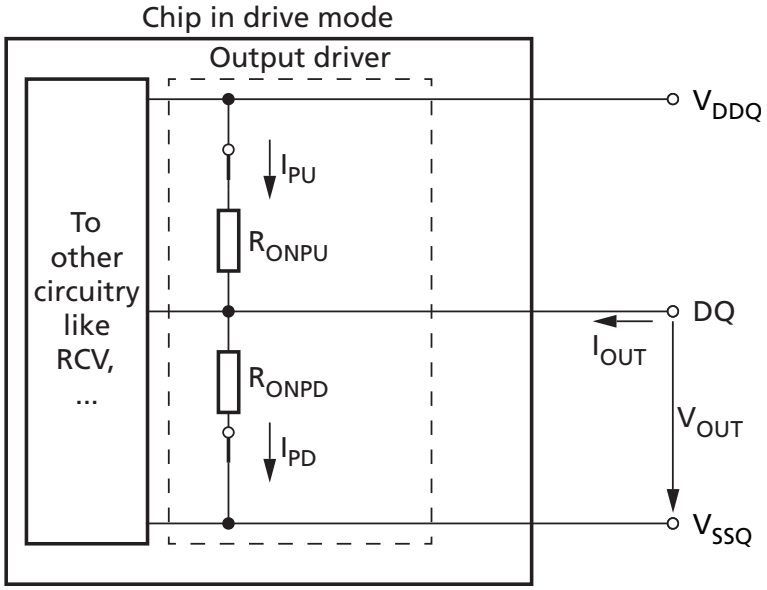
R_{ON,nom_CT}	Resistor	V_{OUT}	Min	Nom	Max	Unit
34Ω	R_{ONPD_CT}	$V_{OB(DC)} = 0.2 \times V_{DDQ}$	N/A	N/A	1.9	$R_{ZQ}/7$
		$V_{OL(DC)} = 0.5 \times V_{DDQ}$	N/A	N/A	2.0	$R_{ZQ}/7$
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	N/A	N/A	2.2	$R_{ZQ}/7$
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	N/A	N/A	2.5	$R_{ZQ}/7$
	R_{ONPU_CT}	$V_{OB(DC)} = 0.2 \times V_{DDQ}$	N/A	N/A	1.9	$R_{ZQ}/7$
		$V_{OL(DC)} = 0.5 \times V_{DDQ}$	N/A	N/A	2.0	$R_{ZQ}/7$
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	N/A	N/A	2.2	$R_{ZQ}/7$
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	N/A	N/A	2.5	$R_{ZQ}/7$

Notes: 1. Assumes R_{ZQ} = 240Ω; ZQ calibration not required.

Output Driver Electrical Characteristics

The DDR4 driver supports two R_{ON} values. These R_{ON} values are referred to as strong mode (low R_{ON}: 34Ω) and weak mode (high R_{ON}: 48Ω). A functional representation of the output buffer is shown in the figure below.

Figure 238: Output Driver: Definition of Voltages and Currents



The output driver impedance, R_{ON}, is determined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON(34)} = R_{ZQ}/7$, or $R_{ON(48)} = R_{ZQ}/5$. This provides either a nominal 34.3Ω ±10% or 48Ω ±10% with nominal R_{ZQ} = 240Ω.

The individual pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}) are defined as follows:

R_{ONPu} when R_{ONPd} is off:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{|I_{OUT}|}$$

Table 123: Strong Mode (34Ω) Output Driver Electrical Characteristics

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Nom	Max	Unit	Notes
34Ω	R_{ON34PD}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.73	1.00	1.10	$R_{ZQ}/7$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.83	1.00	1.10	$R_{ZQ}/7$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.83	1.00	1.25	$R_{ZQ}/7$	1, 2, 3
	R_{ON34PU}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.90	1.00	1.25	$R_{ZQ}/7$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.90	1.00	1.10	$R_{ZQ}/7$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.80	1.00	1.10	$R_{ZQ}/7$	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PUPD}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	10	–	23	%	1, 2, 3, 4, 6, 7
Mismatch between DQ to DQ within byte variation pull-up, MM_{PUdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–	–	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MM_{PDdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	-	–	10	%	1, 2, 3, 4, 6, 7

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Micron recommends calibrating pull-down and pull-up output driver impedances at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at $0.5 \times V_{DDQ}$ and $1.1\ V_{DDQ}$.
4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}:
   Measure both R_{ONPU} and R_{ONPD} at $0.8 \times V_{DDQ}$ separately; $R_{ON,nom}$ is the nominal R_{ON} value:
$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$
6. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:
$$MM_{PUDD} = \frac{R_{ONPU,max} - R_{ONPU,min}}{R_{ON,nom}} \times 100$$
$$MM_{PDDD} = \frac{R_{ONPD,max} - R_{ONPD,min}}{R_{ON,nom}} \times 100$$
7. The lower and upper bytes of a x16 are each treated on a per byte basis.
8. The minimum values are derated by 9% when the device operates between –40°C and 0°C (T_C).

9. Assumes R_{ZQ} = 240Ω; entire operating temperature range after proper ZQ calibration.

Table 124: Weak Mode (48Ω) Output Driver Electrical Characteristics

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Nom	Max	Unit	Notes
48Ω	R_{ON48PD}	$V_{OL(DC)}$ = 0.5 × V_{DDQ}	0.73	1.00	1.10	R_{ZQ}/5	1, 2, 3
		$V_{OM(DC)}$ = 0.8 × V_{DDQ}	0.83	1.00	1.10	R_{ZQ}/5	1, 2, 3
		$V_{OH(DC)}$ = 1.1 × V_{DDQ}	0.83	1.00	1.25	R_{ZQ}/5	1, 2, 3
	R_{ON48PU}	$V_{OL(DC)}$ = 0.5 × V_{DDQ}	0.90	1.00	1.25	R_{ZQ}/5	1, 2, 3
		$V_{OM(DC)}$ = 0.8 × V_{DDQ}	0.90	1.00	1.10	R_{ZQ}/5	1, 2, 3
		$V_{OH(DC)}$ = 1.1 × V_{DDQ}	0.80	1.00	1.10	R_{ZQ}/5	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PUPD}		$V_{OM(DC)}$ = 0.8 × V_{DDQ}	10	–	23	%	1, 2, 3, 4, 6, 7
Mismatch between DQ to DQ within byte variation pull-up, MM_{PUdd}		$V_{OM(DC)}$ = 0.8 × V_{DDQ}	–	–	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MM_{PDdd}		$V_{OM(DC)}$ = 0.8 × V_{DDQ}	–	–	10	%	1, 2, 3, 4, 6, 7

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Micron recommends calibrating pull-down and pull-up output driver impedances at 0.8 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at 0.5 × V_{DDQ} and 1.1 V_{DDQ}.
4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}:
   Measure both R_{ONPU} and R_{ONPD} at 0.8 × V_{DDQ} separately; $R_{ON,nom}$ is the nominal R_{ON} value:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

6. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:

$$MM_{PUDD} = \frac{R_{ONPU,max} - R_{ONPU,min}}{R_{ON,nom}} \times 100$$

$$MM_{PDDD} = \frac{R_{ONPD,max} - R_{ONPD,min}}{R_{ON,nom}} \times 100$$

7. The lower and upper bytes of a x16 are each treated on a per byte basis.
8. The minimum values are derated by 9% when the device operates between –40°C and 0°C (T_C).
9. Assumes R_{ZQ} = 240Ω; entire operating temperature range after proper ZQ calibration

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@ calibration)$; $V_{DD} = V_{DDQ}$

Table 125: Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
R_{ONPU}@ $V_{OH(DC)}$	0.6 - $dR_{ON}dTH \times \lvert\Delta T\rvert$ - $dR_{ON}dVH \times \lvert\Delta V\rvert$	1.1 _ $dR_{ON}dTH \times \lvert\Delta T\rvert$ + $dR_{ON}dVH \times \lvert\Delta V\rvert$	$R_{ZQ}/6$
R_{ON}@ $V_{OM(DC)}$	0.9 - $dR_{ON}dTM \times \lvert\Delta T\rvert$ - $dR_{ON}dVM \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTM \times \lvert\Delta T\rvert$ + $dR_{ON}dVM \times \lvert\Delta V\rvert$	$R_{ZQ}/6$
R_{ONPD}@ $V_{OL(DC)}$	0.6 - $dR_{ON}dTL \times \lvert\Delta T\rvert$ - $dR_{ON}dVL \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTL \times \lvert\Delta T\rvert$ + $dR_{ON}dVL \times \lvert\Delta V\rvert$	$R_{ZQ}/6$

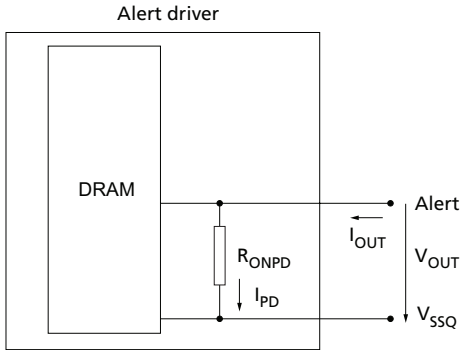
Table 126: Output Driver Voltage and Temperature Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV

Alert Driver

A functional representation of the alert output buffer is shown in the figure below. Output driver impedance, R_{ON}, is defined as follows.

Figure 239: Alert Driver



R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{\lvert I_{OUT} \rvert}$$

Table 127: Alert Driver Voltage

$R_{ON,nom}$	Register	V_{OUT}	Min	Nom	Max	Unit
N/A	R_{ONPD}	$V_{OL(DC)} = 0.1 \times V_{DDQ}$	0.3	N/A	1.2	$R_{ZQ}/7$
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.4	N/A	1.2	$R_{ZQ}/7$
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.4	N/A	1.4	$R_{ZQ}/7$

Notes: 1. V_{DDQ} voltage is at $V_{DDQ(DC)}$.

Electrical Characteristics – On-Die Termination Characteristics

ODT Levels and I-V Characteristics

On-die termination (ODT) effective resistance settings are defined and can be selected by any or all of the following options:

- MR1[10:8] ($R_{TT(NOM)}$): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.
- MR2[11:9] ($R_{TT(WR)}$): Disable, 240 ohms,120 ohms, and 80 ohms.
- MR5[8:6] ($R_{TT(Park)}$): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.

ODT is applied to the following inputs:

- x4: DQ, DM_n, DQS_t, and DQS_c inputs.
- x8: DQ, DM_n, DQS_t, DQS_c, TDQS_t, and TDQS_c inputs.
- x16: DQ, LDM_n, UDM_n, LDQS_t, LDQS_c, UDQS_t, and UDQS_c inputs.

A functional representation of ODT is shown in the figure below.

Figure 240: ODT Definition of Voltages and Currents

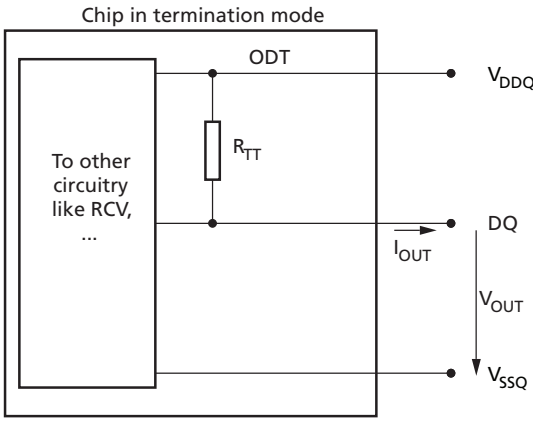


Table 128: ODT DC Characteristics

R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
240 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R_{ZQ}	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R_{ZQ}	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R_{ZQ}	1, 2, 3
120 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/2$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/2$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/2$	1, 2, 3
80 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/3$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/3$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/3$	1, 2, 3

Table 128: ODT DC Characteristics (Continued)

R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
60 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/4$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/4$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/4$	1, 2, 3
48 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1, 2, 3
40 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/6$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/6$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/6$	1, 2, 3
34 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1, 2, 3
DQ-to-DQ mismatch within byte	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0	–	10	%	1, 2, 4, 5, 6

Notes: 1. The tolerance limits are specified after calibration to 240 ohm ±1% resistor with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see ODT Temperature and Voltage Sensitivity.
2. Micron recommends calibrating pull-up ODT resistors at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity specification shown here.
3. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and $V_{SSQ} = V_{SS}$.
4. The DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c.
5. R_{TT} variance range ratio to R_{TT} nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-to-DQ mismatch} = \frac{R_{TT(MAX)} - R_{TT(MIN)}}{R_{TT(NOM)}} \times 100$$

6. DQ-to-DQ mismatch for a x16 device is treated as two separate bytes.
7. For IT, AT, and UT devices, the minimum values are derated by 9% when the device operates between –40°C and 0°C (TC).

ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following equations and tables.

$\Delta T = T - T(@\ \text{calibration})$; $\Delta V = V_{DDQ} - V_{DDQ}(@\ \text{calibration})$; $V_{DD} = V_{DDQ}$

Table 129: ODT Sensitivity Definitions

Parameter	Min	Max	Unit
$R_{TT}@$	$0.9 - dR_{TT}dT \times \lvert\Delta T\rvert - dR_{TT}dV \times \lvert\Delta V\rvert$	$1.6 + dR_{TT}dTH \times \lvert\Delta T\rvert + dR_{TT}dVH \times \lvert\Delta V\rvert$	R_{ZQ}/n

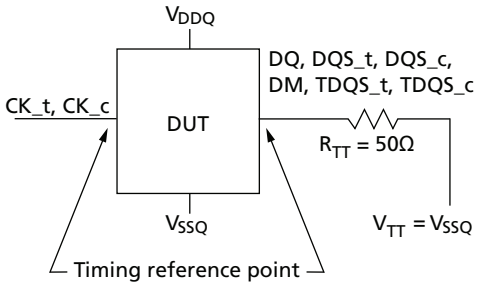
Table 130: ODT Voltage and Temperature Sensitivity

Parameter	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

Figure 241: ODT Timing Reference Load



ODT Timing Definitions and Waveforms

Definitions for ^{t}ADC, ^{t}AONAS, and ^{t}AOFAS are provided in the 4 and shown in 3 and 5. Measurement reference settings are provided in the subsequent 5.

The ^{t}ADC for the dynamic ODT case and read disable ODT cases are represented by ^{t}ADC of Direct ODT Control case.

Table 131: ODT Timing Definitions

Parameter	Begin Point Definition	End Point Definition	Figure
^{t}ADC	Rising edge of CK_t, CK_c defined by the end point of DOD-TLoff	Extrapolated point at $V_{RTT,nom}$	3
	Rising edge of CK_t, CK_c defined by the end point of DOD-TLon	Extrapolated point at V_{SSQ}	3
	Rising edge of CK_t, CK_c defined by the end point of ODTLcnw	Extrapolated point at $V_{RTT,nom}$	4
	Rising edge of CK_t, CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at V_{SSQ}	4
^{t}AONAS	Rising edge of CK_t, CK_c with ODT being first registered HIGH	Extrapolated point at V_{SSQ}	5
^{t}AOFAS	Rising edge of CK_t, CK_c with ODT being first registered LOW	Extrapolated point at $V_{RTT,nom}$	5

Table 132: Reference Settings for ODT Timing Measurements

Measure Parameter	$R_{TT(Park)}$	$R_{TT(NOM)}$	$R_{TT(WR)}$	VSW1	VSW2	Note
^{t}ADC	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 4
	–	$R_{ZQ}/7$ (34Ω)	High-Z	0.20V	0.40V	1, 3, 5
^{t}AONAS	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 6
^{t}AOFAS	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 6

Notes: 1. MR settings are as follows: MR1 has A10 = 1, A9 = 1, A8 = 1 for $R_{TT(NOM)}$ setting; MR5 has A8 = 0, A7 = 0, A6 = 0 for $R_{TT(Park)}$ setting; and MR2 has A11 = 0, A10 = 1, A9 = 1 for $R_{TT(WR)}$ setting.
2. ODT state change is controlled by ODT pin.
3. ODT state change is controlled by a WRITE command.
4. Refer to Figure 3.
5. Refer to Figure 4.
6. Refer to Figure 5.

Figure 242: ^{t}ADC Definition with Direct ODT Control

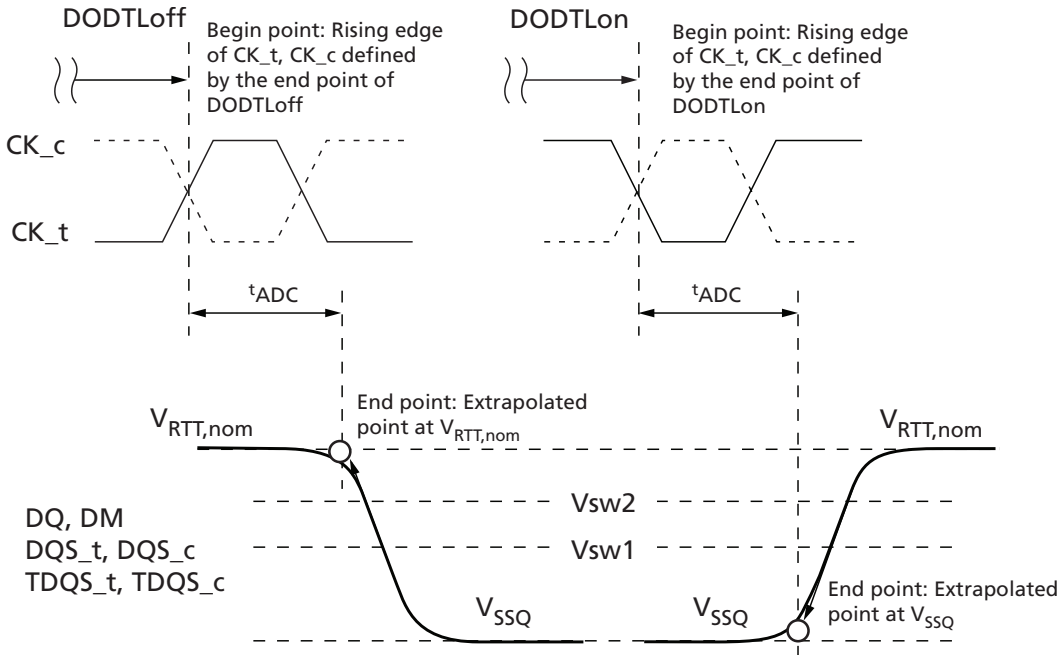


Figure 243: ^{t}ADC Definition with Dynamic ODT Control

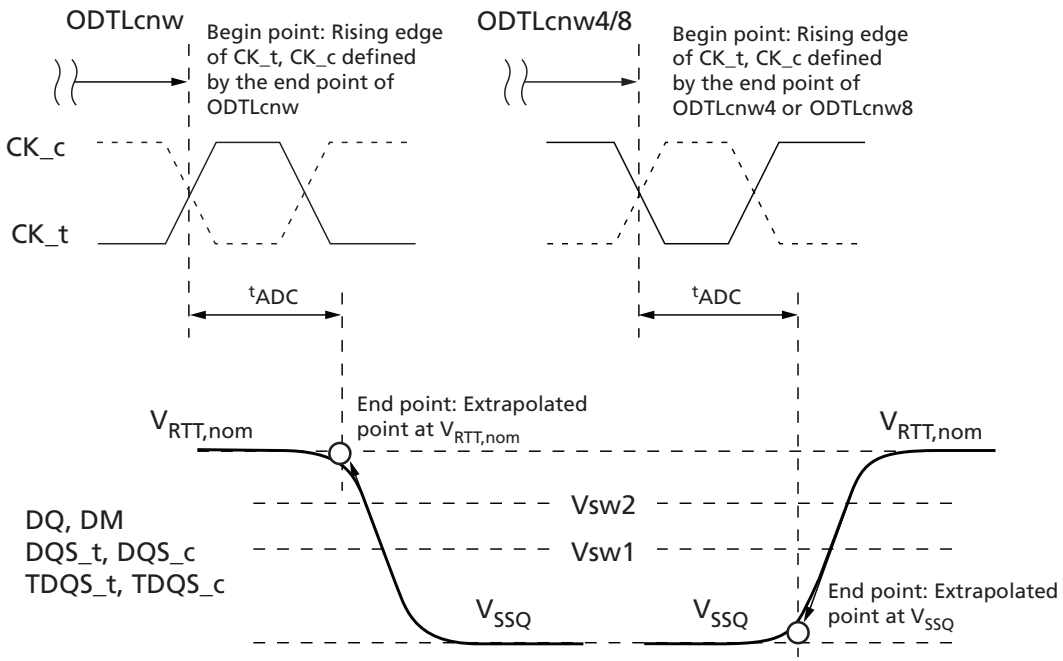


Figure 244: ^{t}AOFAS and ^{t}AONAS Definitions