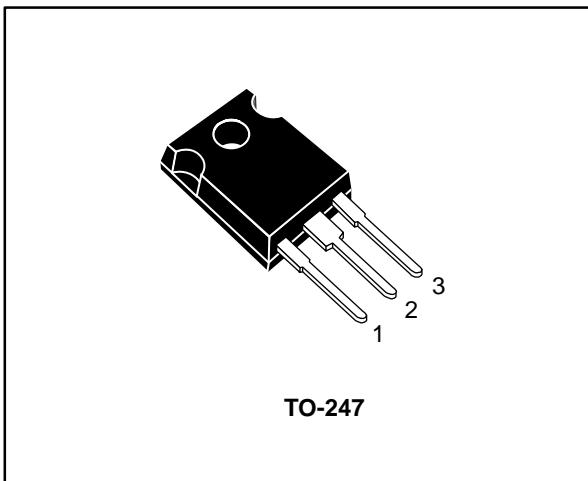
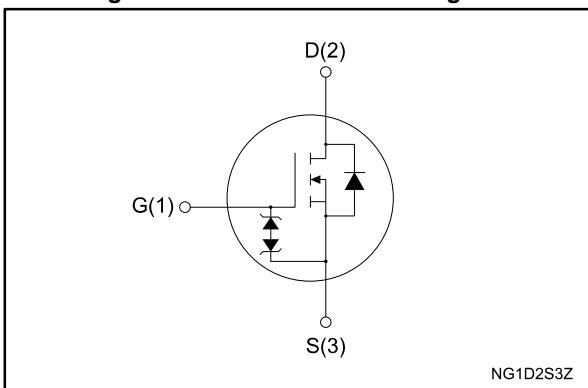


## N-channel 650 V, 0.058 Ω typ., 48 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data



**Figure 1: Internal schematic diagram**



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STW56N65DM2	650 V	0.065 Ω	48 A	360 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

**Table 1: Device summary**

Order code	Marking	Package	Packing
STW56N65DM2	56N65DM2	TO-247	Tube

**Contents**

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
4.1	TO-247 package information.....	9
<b>5</b>	<b>Revision history .....</b>	<b>11</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25^\circ C$	48	A
	Drain current (continuous) at $T_{case} = 100^\circ C$	30	
$I_{DM}^{(1)}$	Drain current (pulsed)	192	A
$P_{TOT}$	Total dissipation at $T_{case} = 25^\circ C$	360	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
$T_{stg}$	Storage temperature	-55 to 150	$^\circ C$
$T_j$	Operating junction temperature		

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 48$  A,  $dI/dt = 900$  A/ $\mu$ s;  $V_{DS}$  peak <  $V_{(BR)DSS}$ ,  $V_{DD} = 400$  V(3)  $V_{DS} \leq 520$  V.**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.35	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive	7	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	1300	mJ

**Notes:**(1) starting  $T_j = 25^\circ C$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50$  V.

## 2 Electrical characteristics

( $T_{case} = 25^\circ C$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V, I_D = 1 mA$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0 V, V_{DS} = 650 V$			10	$\mu A$
		$V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125^\circ C$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			$\pm 5$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 24 A$		0.058	0.065	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V$	-	4100	-	pF
$C_{oss}$	Output capacitance		-	160	-	
$C_{rss}$	Reverse transfer capacitance		-	2.5	-	
$C_{oss\ eq.\ (1)}$	Equivalent output capacitance	$V_{DS} = 0$ to $520 V, V_{GS} = 0 V$	-	375	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 MHz, I_D = 0 A$	-	4.1	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520 V, I_D = 48 A, V_{GS} = 10 V$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	88	-	nC
$Q_{gs}$	Gate-source charge		-	22	-	
$Q_{gd}$	Gate-drain charge		-	37	-	

**Notes:**

<sup>(1)</sup>  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 V, I_D = 24 A$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	28	-	ns
$t_r$	Rise time		-	31	-	
$t_{d(off)}$	Turn-off delay time		-	157	-	
$t_f$	Fall time		-	7.7	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		48	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		192	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 48 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 48 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 100 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	135		ns
$Q_{rr}$	Reverse recovery charge		-	0.68		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	10		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 48 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	260		ns
$Q_{rr}$	Reverse recovery charge		-	2.75		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	21		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1

## Electrical characteristics (curves)

Figure 2: Safe operating area

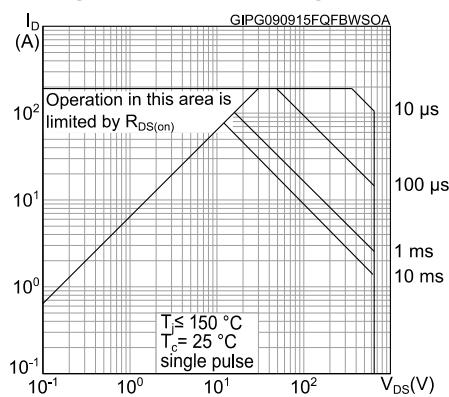


Figure 3: Thermal impedance

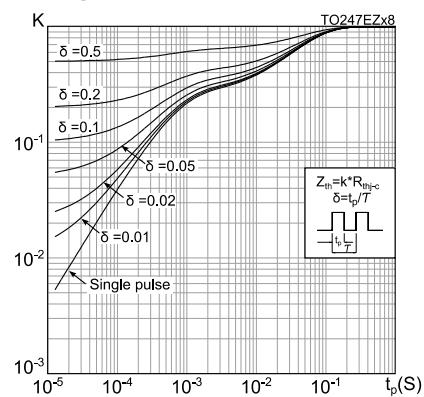


Figure 4: Output characteristics

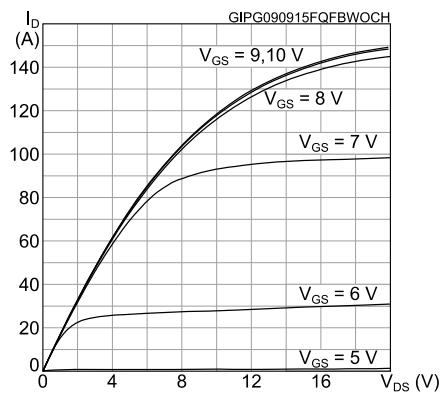


Figure 5: Transfer characteristics

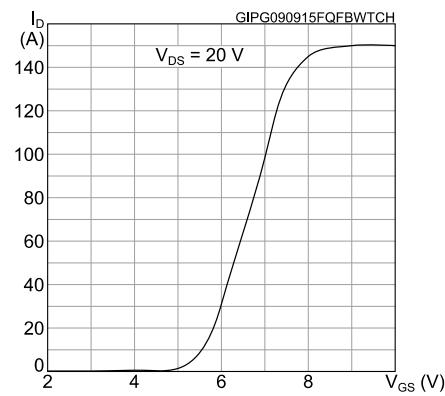


Figure 6: Gate charge vs gate-source voltage

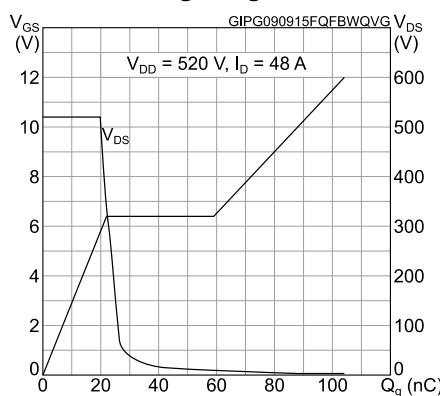
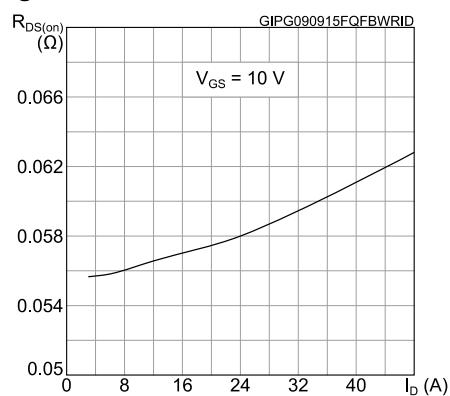
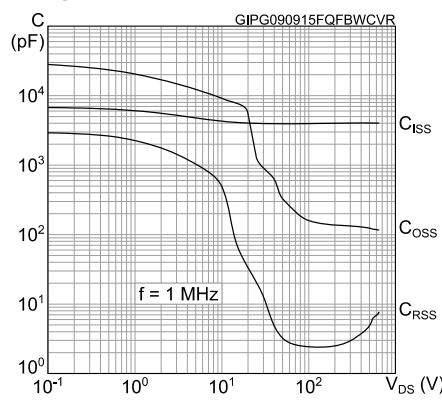
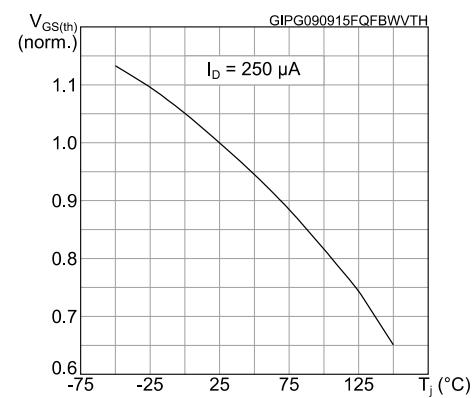
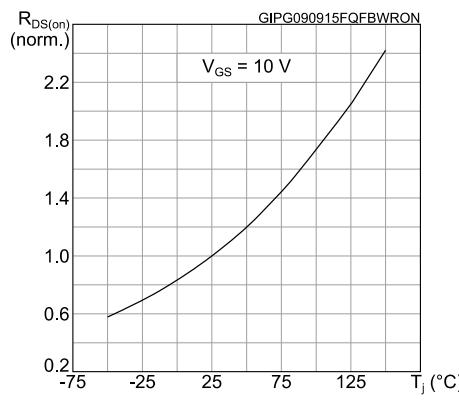
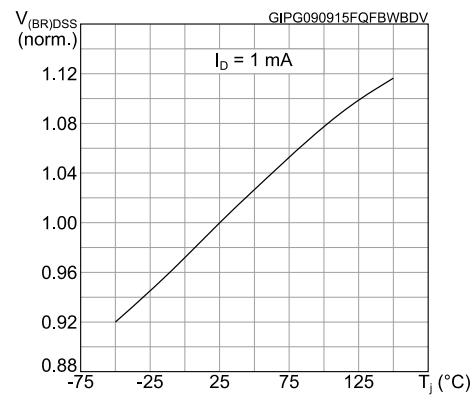
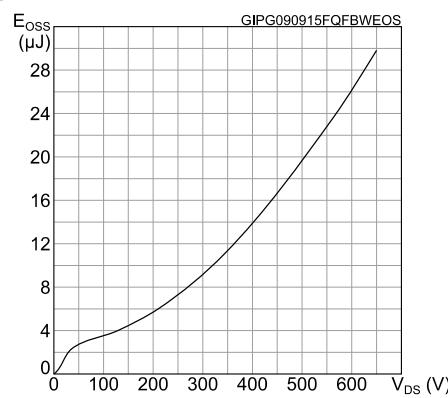
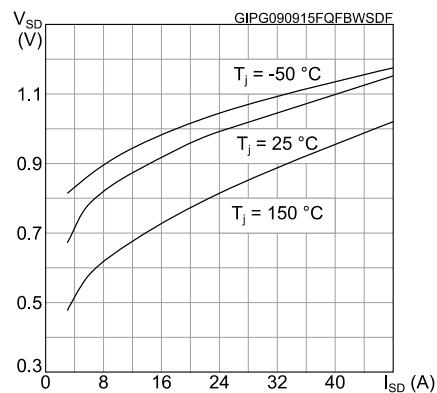


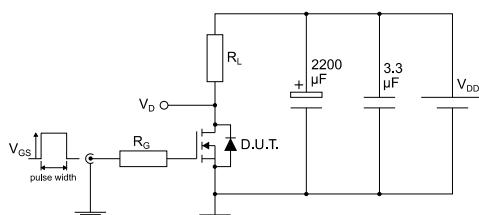
Figure 7: Static drain-source on-resistance



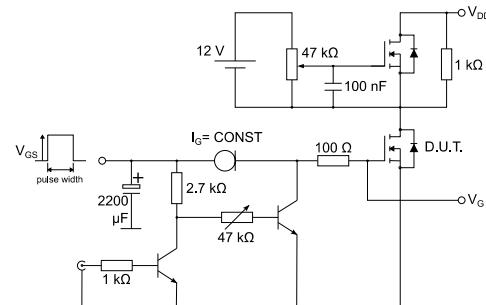
**Figure 8: Capacitance variations****Figure 9: Normalized gate threshold voltage vs temperature****Figure 10: Normalized on-resistance vs temperature****Figure 11: Normalized V(BR)DSS vs temperature****Figure 12: Output capacitance stored energy****Figure 13: Source- drain diode forward characteristics**

### 3 Test circuits

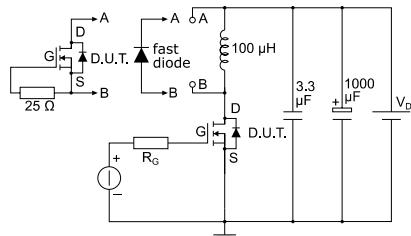
**Figure 14: Test circuit for resistive load switching times**



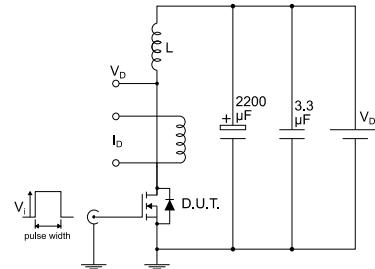
**Figure 15: Test circuit for gate charge behavior**



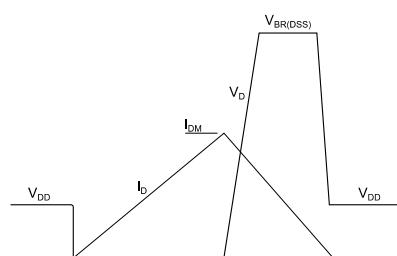
**Figure 16: Test circuit for inductive load switching and diode recovery times**



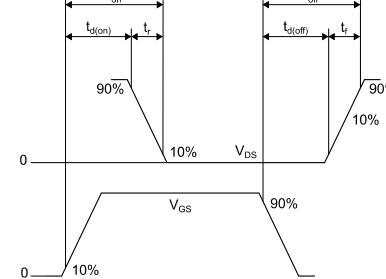
**Figure 17: Unclamped inductive load test circuit**



**Figure 18: Unclamped inductive waveform**



**Figure 19: Switching time waveform**



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 20: TO-247 package outline

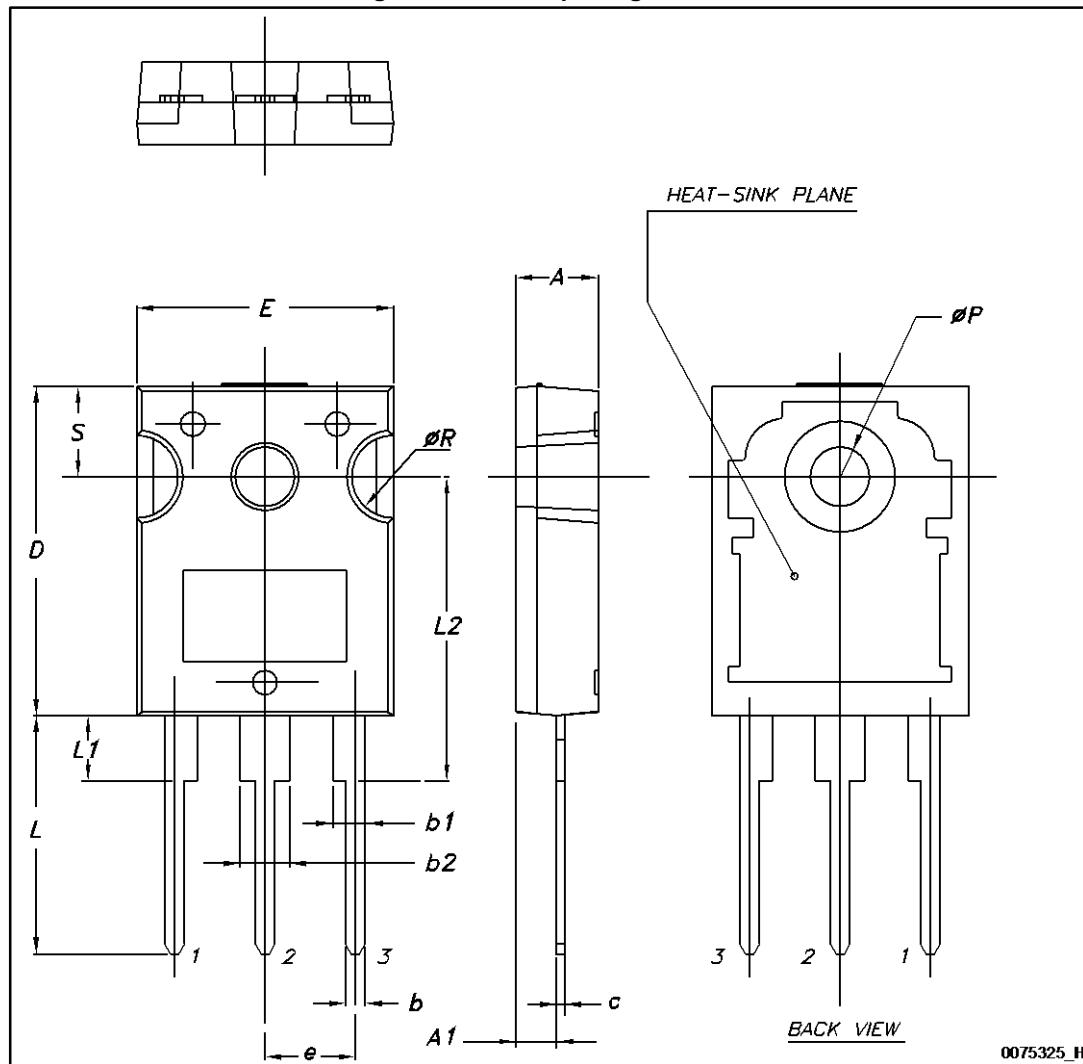


Table 9: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
27-Nov-2014	1	First release.
15-Sep-2015	2	<p>Text and formatting changes throughout document.</p> <p>In section <i>Electrical ratings</i>:</p> <ul style="list-style-type: none"><li>- updated tables <i>Absolute maximum ratings</i> and <i>Avalanche characteristics</i></li></ul> <p>In section <i>Electrical characteristics</i>:</p> <ul style="list-style-type: none"><li>- updated and renamed table <i>Static</i> (was On/off states)</li><li>- updated tables <i>Dynamic</i>, <i>Switching times</i> and <i>Source-drain diode</i></li></ul> <p>Updated section <i>Electrical characteristics (curves)</i></p>

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