DDR4 SDRAM

MT40A2G4
MT40A1G8
MT40A512M16

Features

- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- Refresh time of 8192-cycle at T_C temperature range:
  - 64ms at -40°C to 85°C
  - 32ms at >85°C to 95°C
  - 16ms at >95°C to 105°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability
- MBIST-PPR support (Die Revision R only)

Options[1]	Marking
• Configuration	
– 2 Gig x 4	2G4
– 1 Gig x 8	1G8
– 512 Meg x 16	512M16
• 78-ball FBGA package (Pb-free) – x4, x8	
– 9mm x 13.2mm – Rev. A	PM
– 8mm x 12mm – Rev. B, D, G	WE
– 7.5mm x 11mm – Rev. E, H, J, R	SA
• 96-ball FBGA package (Pb-free) – x16	
– 9mm x 14mm – Rev. A	HA
– 8mm x 14mm – Rev. B	JY
– 7.5mm x 13.5mm – Rev. D, E, H	LY
– 7.5mm x 13mm – Rev. J, R	TB
• Timing – cycle time	
– 0.625ns @ CL = 22 (DDR4-3200)	-062E
– 0.682ns @ CL = 21 (DDR4-2933)	-068
– 0.750ns @ CL = 19 (DDR4-2666)	-075
– 0.750ns @ CL = 18 (DDR4-2666)	-075E
– 0.833ns @ CL = 17 (DDR4-2400)	-083
– 0.833ns @ CL = 16 (DDR4-2400)	-083E
– 0.937ns @ CL = 15 (DDR4-2133)	-093E
– 1.071ns @ CL = 13 (DDR4-1866)	-107E
• Operating temperature	
– Commercial (0° ≤ T_C ≤ 95°C)	None
– Industrial (–40° ≤ T_C ≤ 95°C)	IT
– Automotive (–40° ≤ T_C ≤ 105°C)	AT
• Revision	:A, :B, :D, :E, :G, :H, :J, :R

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^tAA (ns)	^tRCD (ns)	^tRP (ns)
-062Y	3200	22-22-22	13.75 (13.32)	13.75 (13.32)	13.75 (13.32)
-062E	3200	22-22-22	13.75	13.75	13.75
-068	2933	21-21-21	14.32 (13.75)	14.32 (13.75)	14.32 (13.75)
-075E	2666	18-18-18	13.50	13.50	13.50

Table 1: Key Timing Parameters (Continued)

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^{t}AA (ns)	^{t}RCD (ns)	^{t}RP (ns)
-075	2666	19-19-19	14.25 (13.75)	14.25 (13.75)	14.25 (13.75)
-083E	2400	16-16-16	13.32	13.32	13.32
-083	2400	17-17-17	14.16 (13.75)	14.16 (13.75)	14.16 (13.75)
-093E	2133	15-15-15	14.06 (13.50)	14.06 (13.50)	14.06 (13.50)
-093	2133	16-16-16	15.00	15.00	15.00
-107E	1866	13-13-13	13.92 (13.50)	13.92 (13.50)	13.92 (13.50)

Notes: 1. Refer to the Speed Bin Tables for additional details.

Table 2: Addressing

Parameter	2048 Meg x 4	1024 Meg x 8	512 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	128K (A[16:0])	64K (A[15:0])	64K (A[15:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Figure 1: Order Part Number Example

Example Part Number: MT40A1G8SA-062E:R

Configuration	
2 Gig x 4	2G8
1 Gig x 8	1G8
512 Meg x 16	512M16

Die Revision
:A, :B, :D, :G, :E, :H, :J, :R

Case Temperature	Mark
Commercial	None
Industrial	IT
Extended	AT

Package	Mark
78-ball 9.0mm x 13.2mm FBGA	PM
78-ball 8.0mm x 12.0mm FBGA	WE
78-ball 7.5mm x 11.0mm FBGA	SA
96-ball 9.0mm x 14.0mm FBGA	HA
96-ball 8.0mm x 14.0mm FBGA	JY
96-ball 7.5mm x 13.5mm FBGA	LY
96-ball 7.5mm x 13.0mm FBGA	TB

Speed Grade	Cycle Time, CAS Latency
-107E	^{t}CK = 1.071ns, CL = 13
-093E	^{t}CK = 0.937ns, CL = 15
-083E	^{t}CK = 0.833ns, CL = 16
-083	^{t}CK = 0.833ns, CL = 17
-075E	^{t}CK = 0.750ns, CL = 18
-075	^{t}CK = 0.750ns, CL = 19
-068	^{t}CK = 0.682ns, CL = 21
-062E	^{t}CK = 0.625ns, CL = 22

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Important Notes and Warnings

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General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an 8*n*-prefetch architecture to achieve high-speed operation. The 8*n*-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8*n*-bit wide, four-clock data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below –40°C or above 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between –40°C and 0°C.

Automotive Temperature

The automotive temperature (AT) device option requires that the case temperature not exceed below –40°C or above 105°C. The specifications require the refresh rate to 2X when T_C exceeds 85°C; 4X when T_C exceeds 95°C. Additionally, ODT resistance and the input/output impedance must be derated when operating temperature Tc <0°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.
- Not all features described within this document may be available on the Rev. A (first) version.

- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every 8192 × ^{t}REFI. However, in the event CKE is fixed HIGH, toggling CS_n at least once every 8192 × ^{t}REFI is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS_t to VDDQ or VSS/ VSSQ via a resistor in the 200Ω range.
  - Connect UDQS_c to the opposite rail via a resistor in the same 200Ω range.
  - Connect UDM to VDDQ via a large (10,000Ω) pull-up resistor.
  - Connect UDBI to VDDQ via a large (10,000Ω) pull-up resistor.
  - Connect DQ [15:8] individually to VDDQ via a large (10,000Ω) resistors, or float DQ [15:8] .

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tri-state depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.
- The specification requires 8,192 refresh commands within 64ms between 0°C and 85°C. This allows for a ^{t}REFI of 7.8125µs (the use of "7.8µs" is truncated from 7.8125µs). The specification also requires 8,192 refresh commands within 32ms between 85°C and 95°C. This allows for a ^{t}REFI of 3.90625µs (the use of "3.9µs" is truncated from 3.90625µs).

Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 2: 2 Gig x 4 Functional Block Diagram

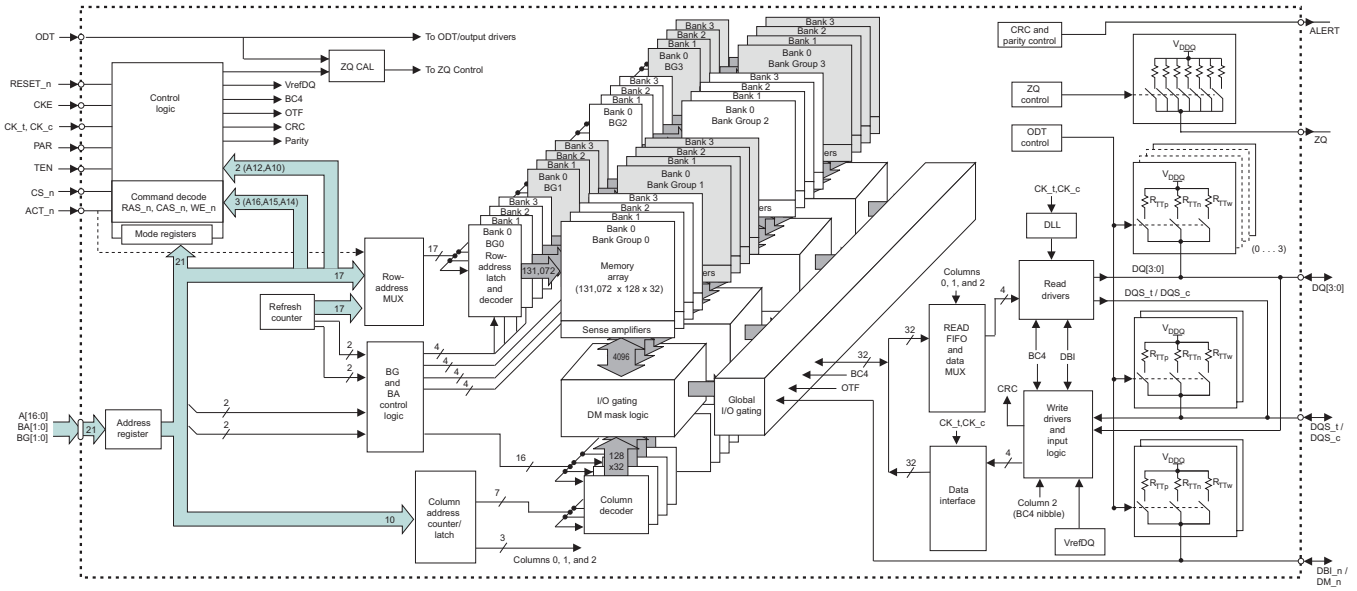


Figure 3: 1 Gig x 8 Functional Block Diagram

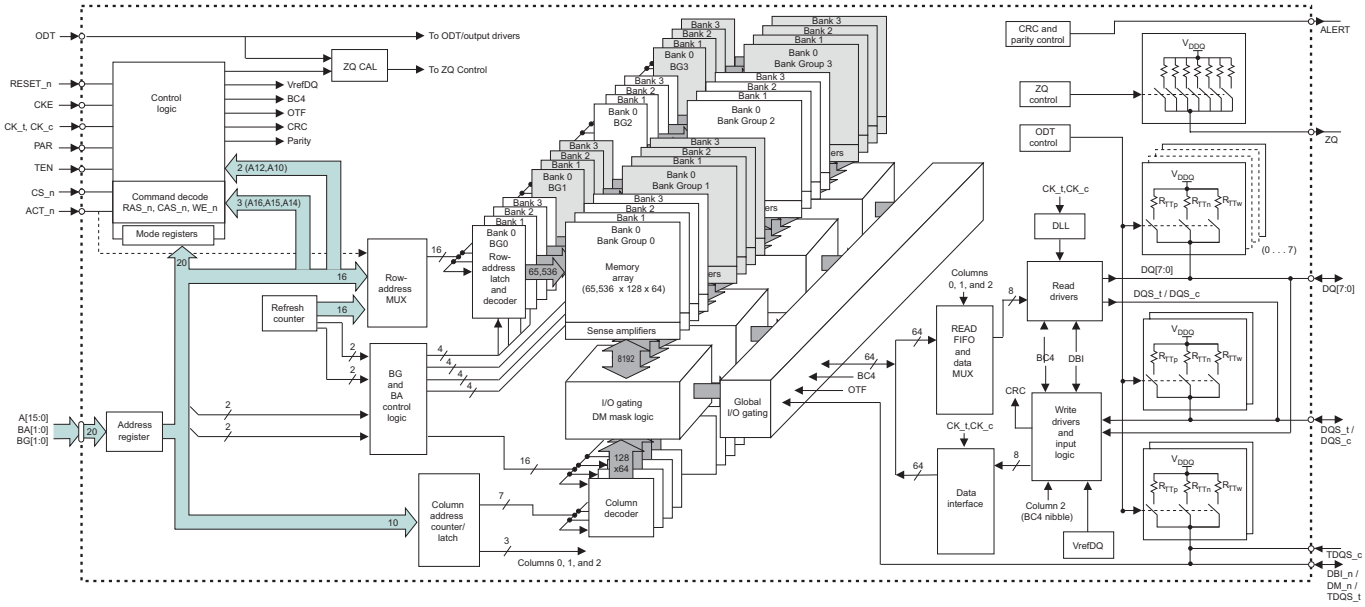
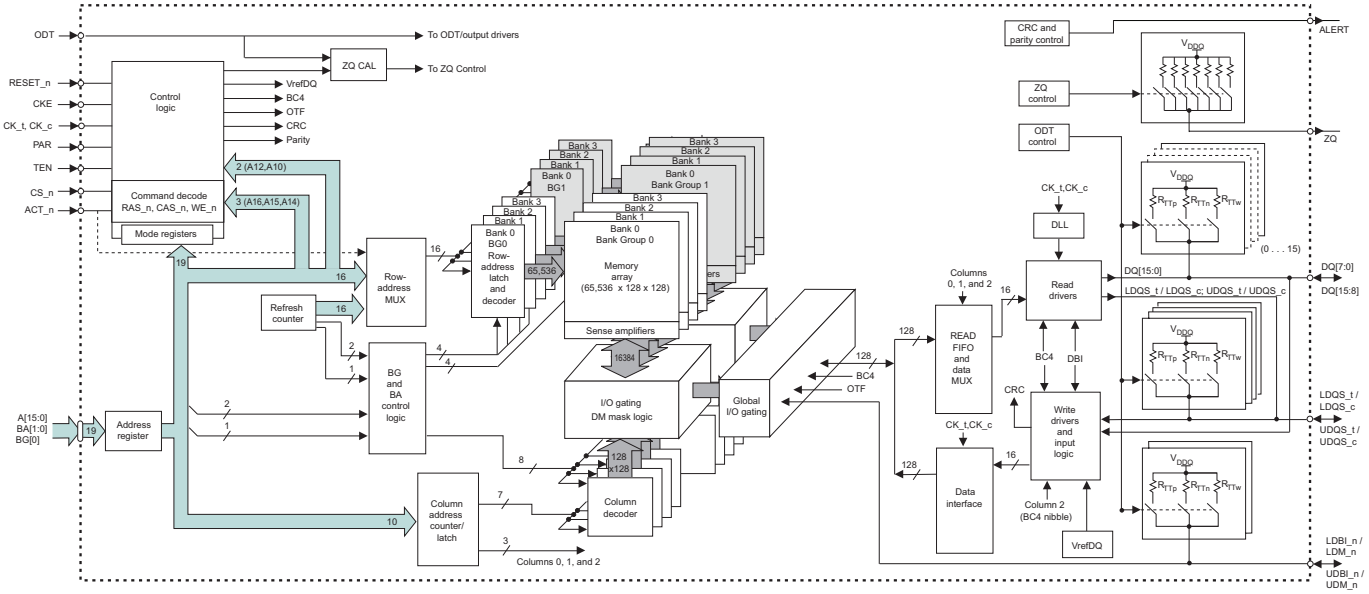
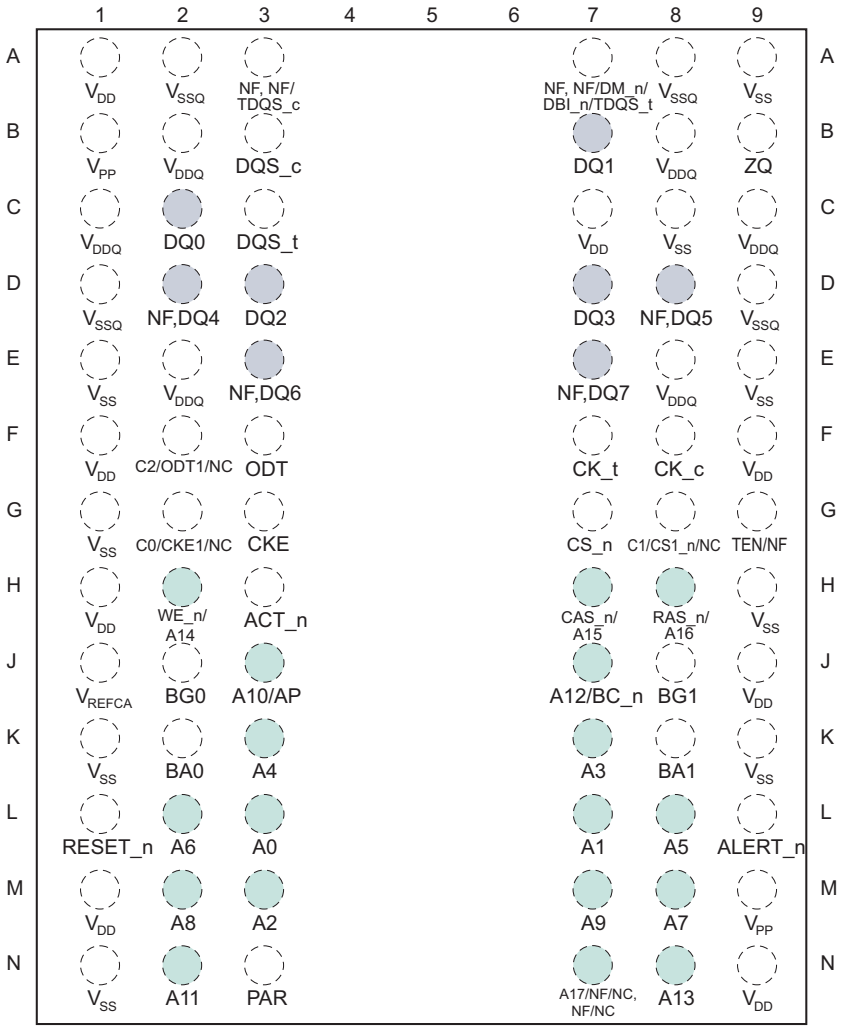


Figure 4: 512 Meg x 16 Functional Block Diagram



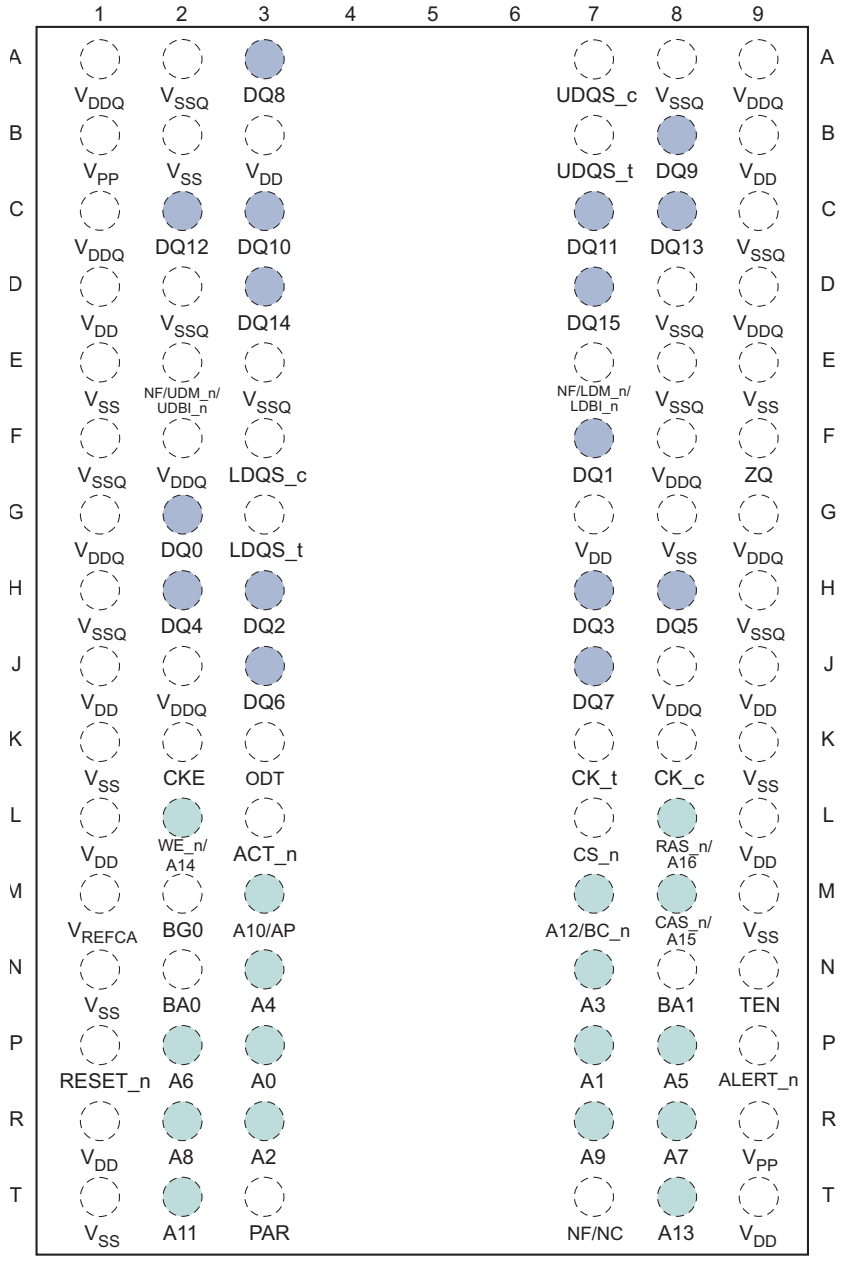
Ball Assignments

Figure 5: 78-Ball x4, x8 Ball Assignments



Notes: 1. See Ball Descriptions.
2. A comma "," separates the configuration; a slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Figure 6: 96-Ball x16 Ball Assignments



Notes: 1. See Ball Descriptions.
2. A slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts. A17 connection is part-number specific; Contact vendor for more information.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration, and are NC on the x4/x8 SDP). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

Table 3: Ball Descriptions (Continued)

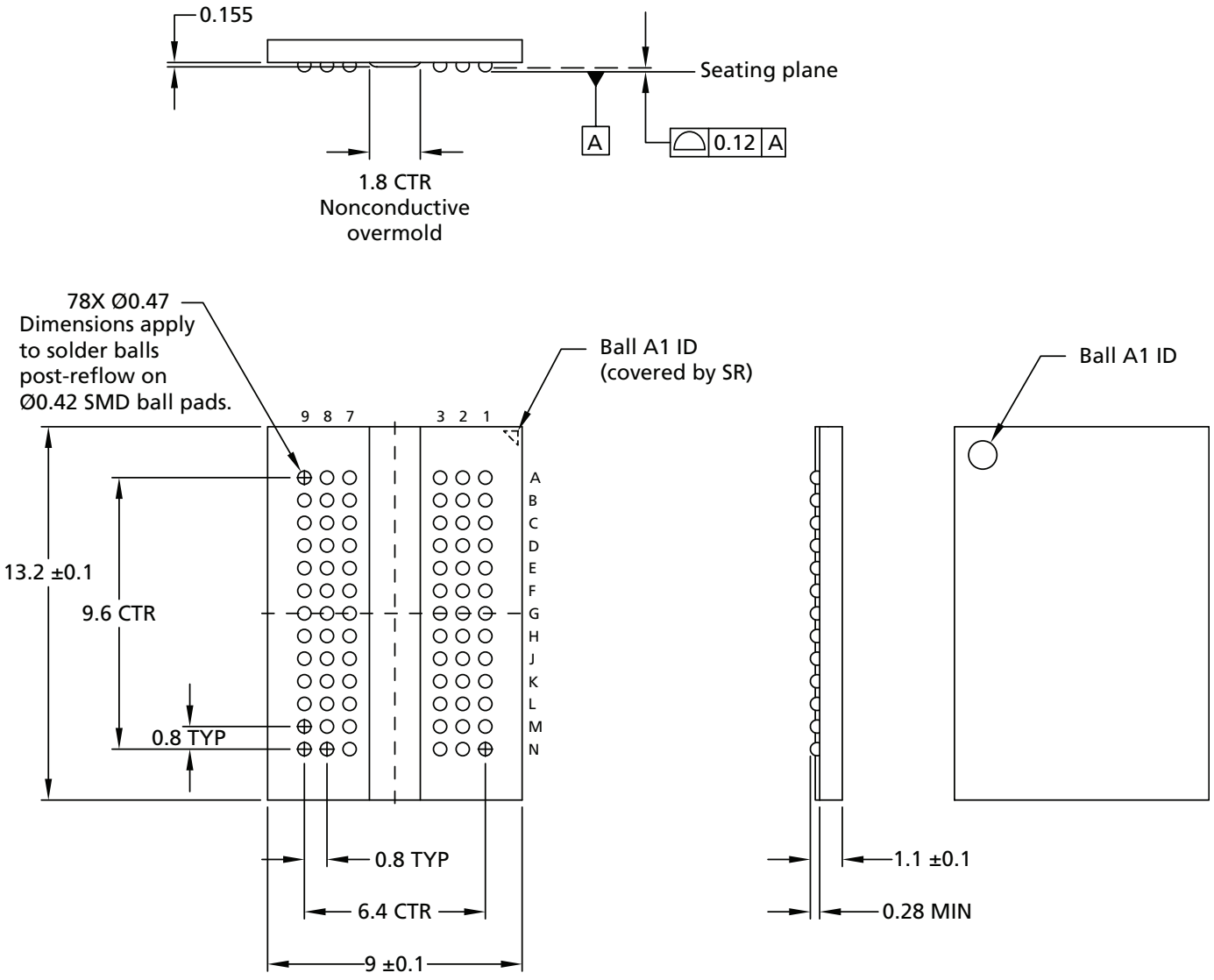
Symbol	Type	Description
CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit, however, timing parameters such as ^{t}XS are still calculated from the first rising clock edge where CKE HIGH satisfies ^{t}IS. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, UDQS_t, UDQS_c, LDQS_t, LDQS_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PAR	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960 mV for DC HIGH and 240 mV for DC LOW).
TEN	Input	**Connectivity test mode:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW). On Micron 3DS devices, connectivity test mode is not supported and the TEN pin should be considered NF maintained LOW at all times.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
DQ	I/O	**Data input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n, UDBI_n, LDBI_n	I/O	**DBI input/output:** Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI is not supported for 3DS devices and should be disabled in MR5. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.
DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	I/O	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	**Termination data strobe:** TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V_{DD}	Supply	**Power supply:** 1.2V ±0.060V.
V_{DDQ}	Supply	**DQ power supply:** 1.2V ±0.060V.
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V/+0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
ZQ	Reference	**Reference ball for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** Internal connection is present but has no function.

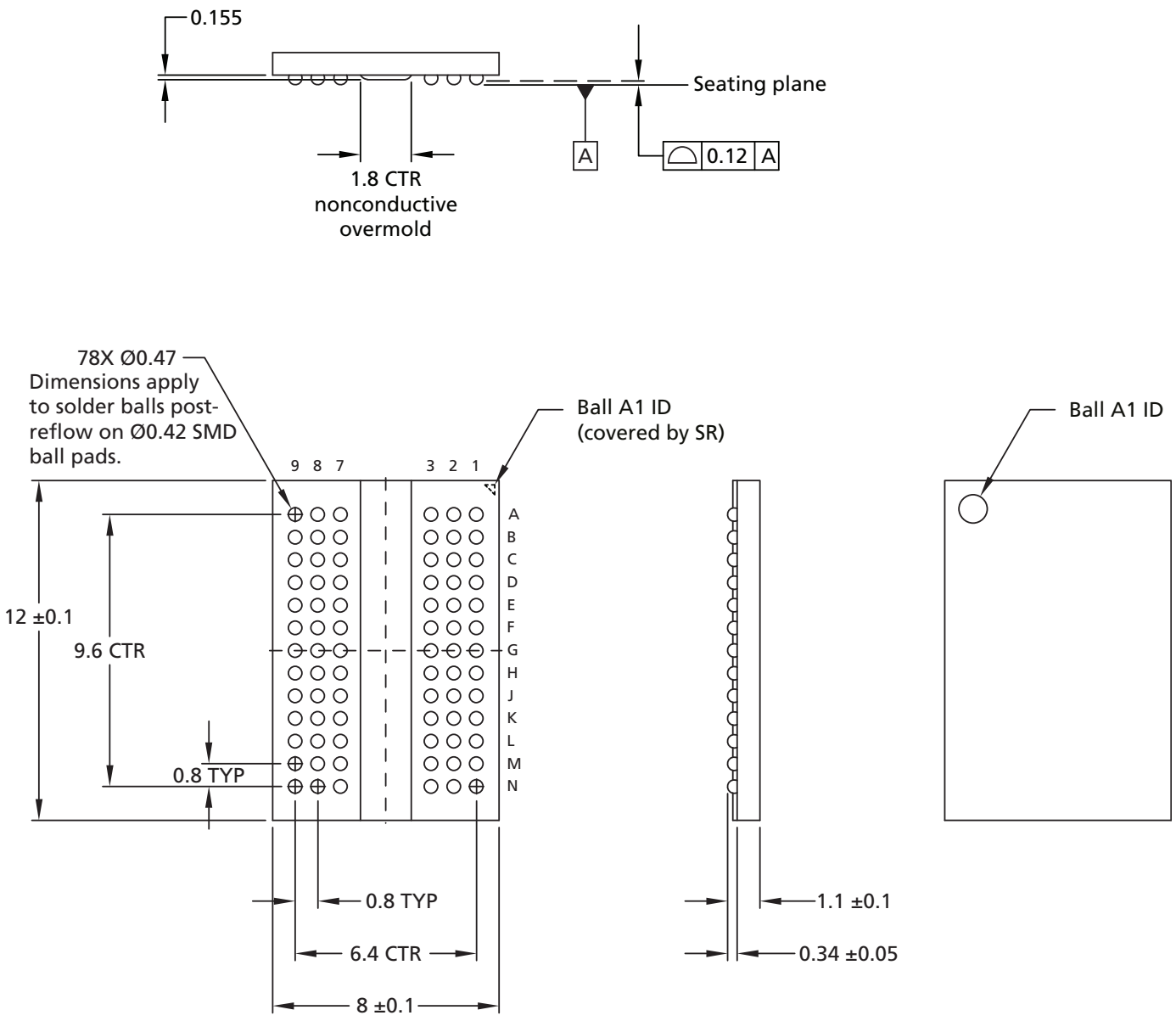
Package Dimensions

Figure 7: 78-Ball FBGA – x4, x8 (PM)



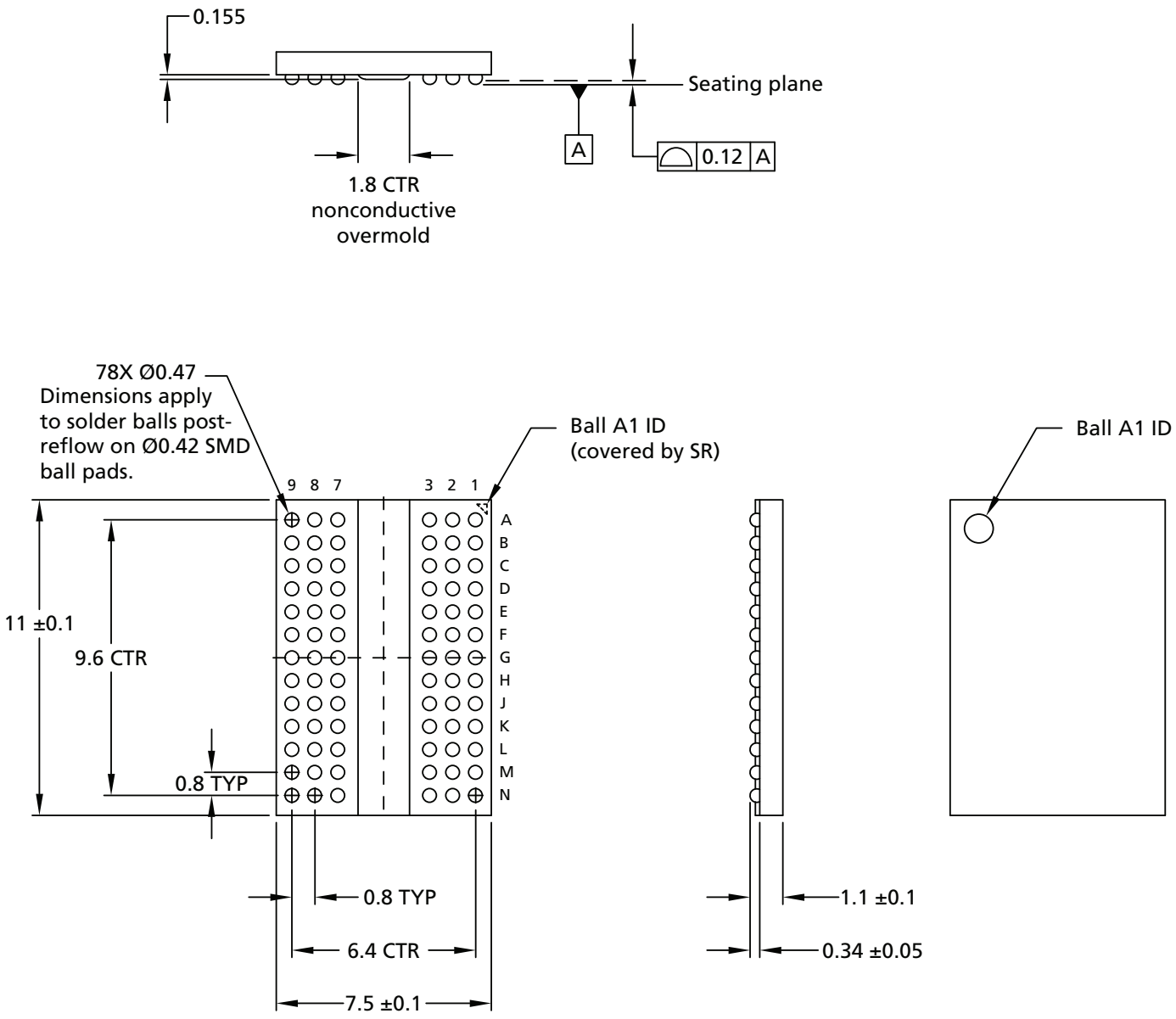
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 8: 78-Ball FBGA – x4, x8 (WE)



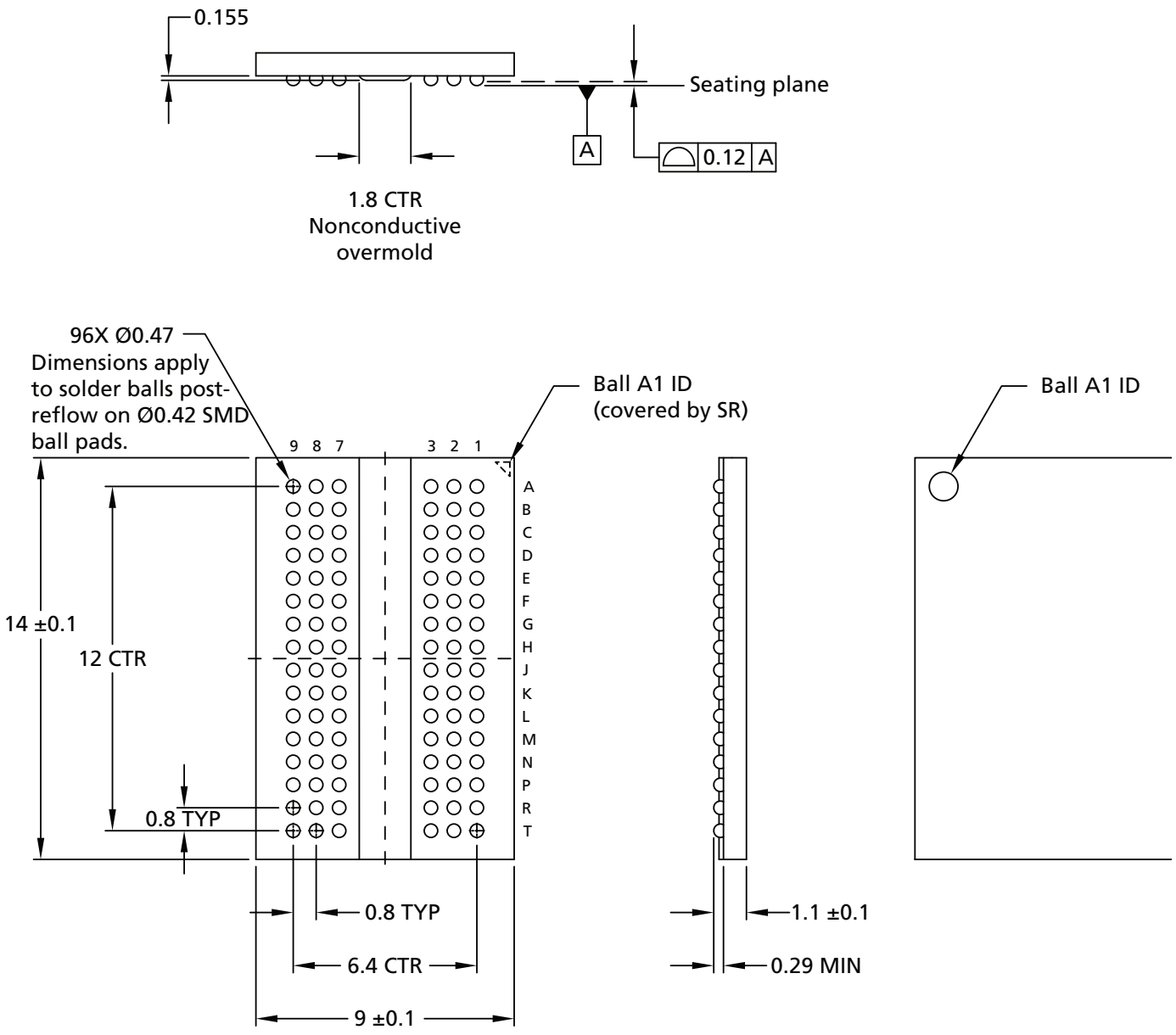
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 9: 78-Ball FBGA – x4, x8 (SA)



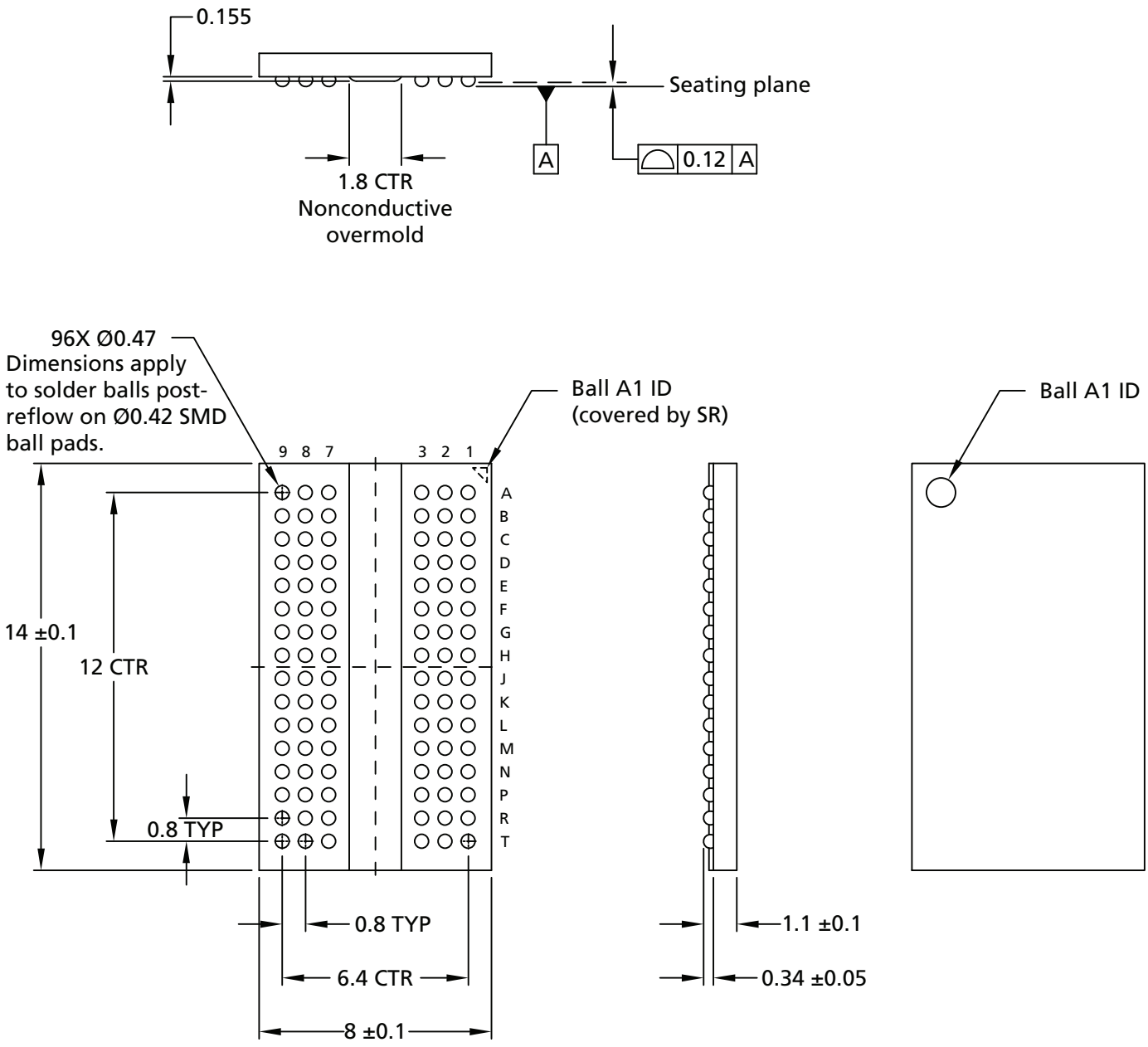
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: Die Revision E, H,J: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).
Solder ball material: Die Revision R: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 10: 96-Ball FBGA – x16 (HA)



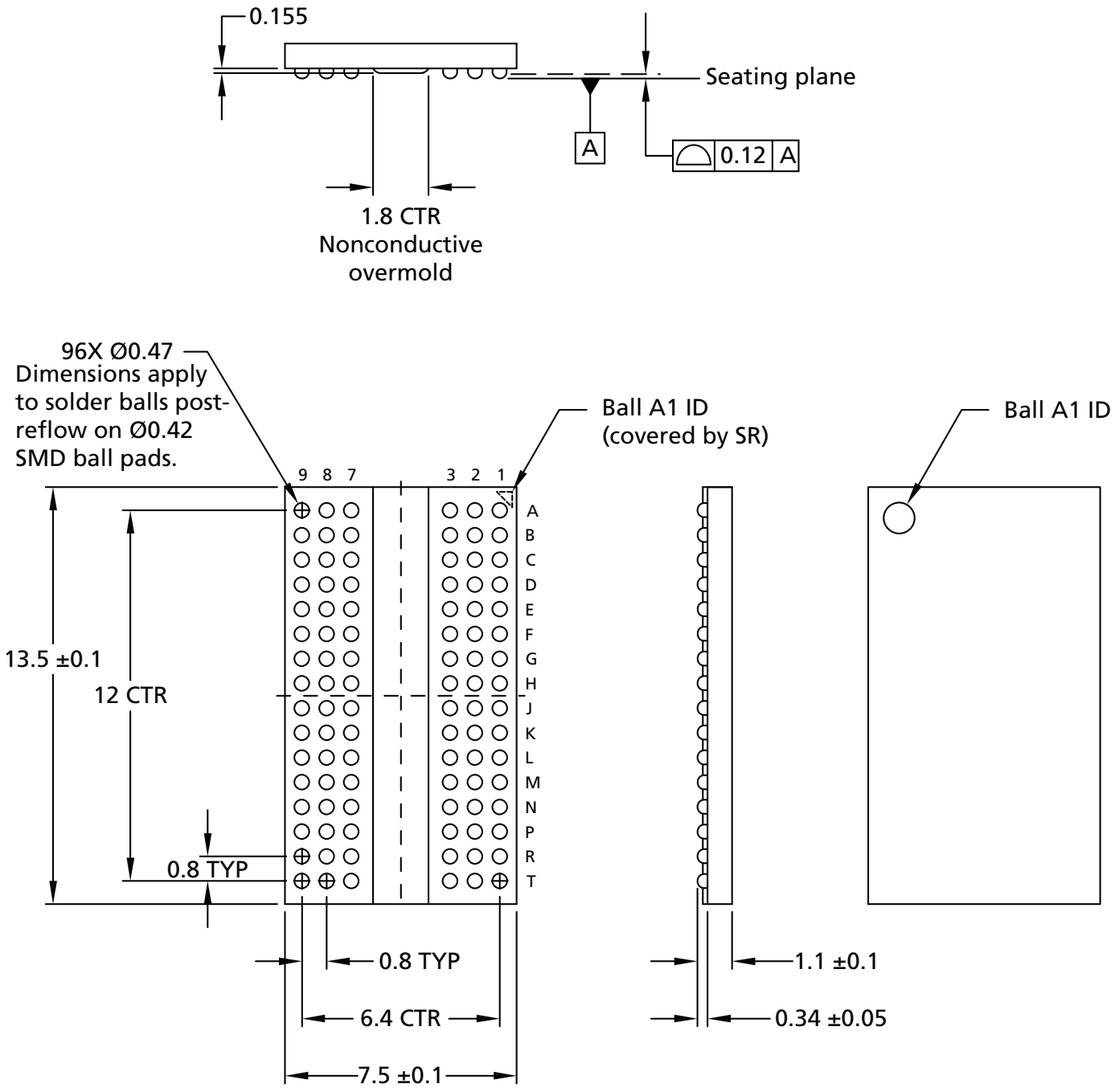
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 11: 96-Ball FBGA – x16 (JY)



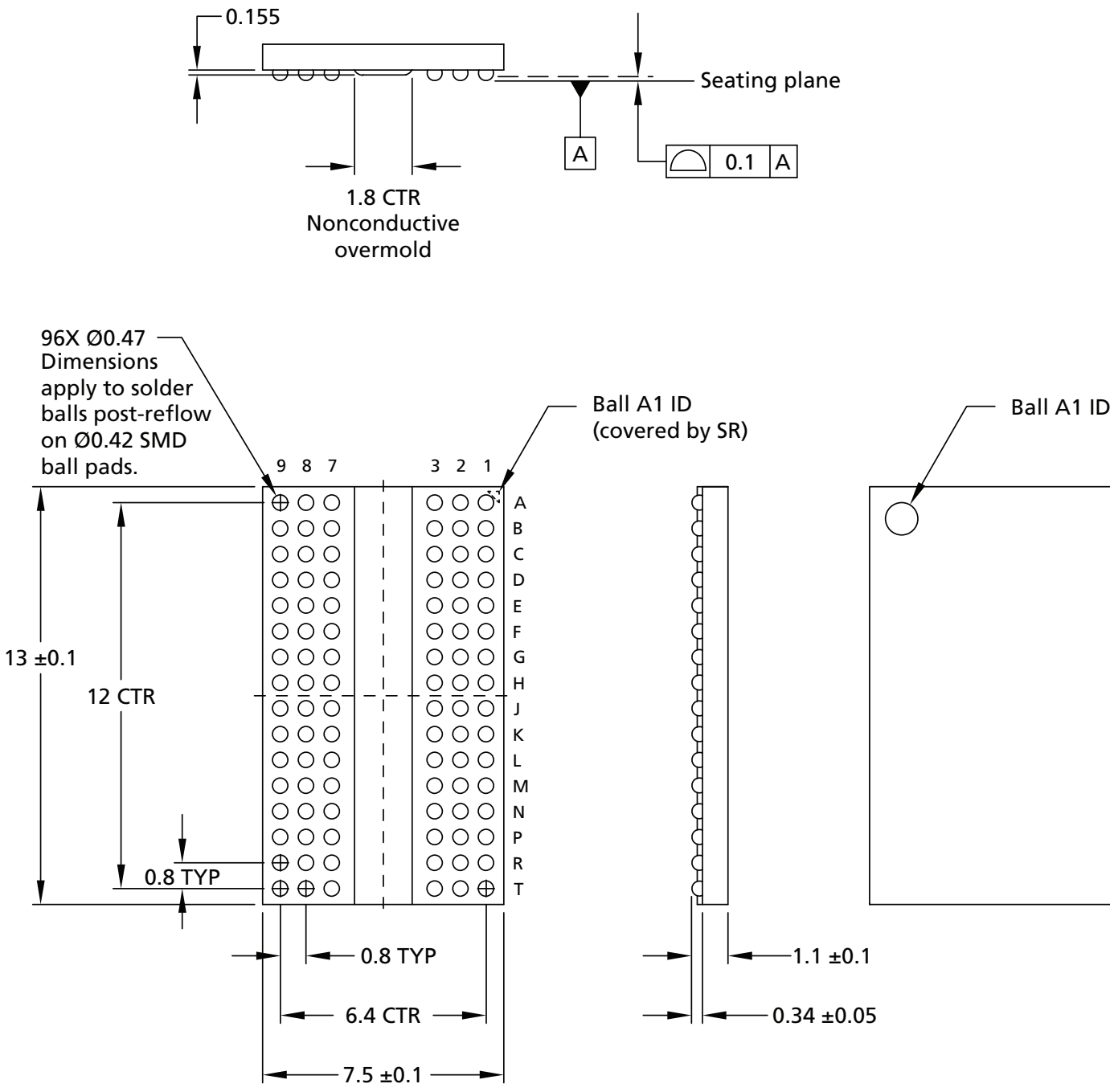
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 12: 96-Ball FBGA – x16 (LY)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 13: 96-Ball FBGA – x16 (TB)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: Die Revision J: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).
Solder ball material: Die Revision R: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

State Diagram

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 14: Simplified State Diagram

Table 4: State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Notes: 1. See the Command Truth Table for more details.

Functional Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x4/x8 devices, and as eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8*n*-bit-wide, four-clock-cycle-data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x4/x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[17:0] select the row. See the Addressing section for more details). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

NOTE: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.

RESET and Initialization Procedure

To ensure proper device function, the power-up and reset initialization default values for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable
- Hard post package repair mode (MR4 A[13]): 0 = disable
- Soft post package repair mode (MR4 A[5]): 0 = disable

Power-Up and Initialization Sequence

The following sequence is required for power-up and initialization:

1. Apply power (RESET_n and TEN should be maintained below 0.2 × V_{DD} while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, RESET_n must be maintained below 0.2 × V_{DD} for a minimum of ^{t}PW_RESET_L and TEN must be maintained below 0.2 × V_{DD} for a minimum of 700µs. CKE is pulled LOW anytime before RESET_n is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and (V_{DD} - V_{DDQ}) < 0.3V. V_{PP} must ramp at the same time or up to 10 minutes prior to V_{DD}, and V_{PP} must be equal to or higher than V_{DD} at all times. The total time for which V_{PP} is powered and V_{DD} is unpowered should not exceed 360 cumulative hours. After V_{DD} has ramped and reached a stable level, RESET_n must go high within 10 minutes. After RESET_n goes high, the initialization sequence must be started within 3 seconds. For debug purposes, the 10 minute and 3 second delay limits may be extended to 60 minutes each provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.
   During power-up, the supply slew rate is governed by the limits stated in the table below and either condition A or condition B listed below must be met.

Table 5: Supply Power-up Slew Rate

Symbol	Min	Max	Unit	Comment
V_{DD}_SL, V_{DDQ}_SL, V_{PP}_SL	0.004	600	V/ms	Measured between 300mV and 80% of supply minimum
V_{DD}_ona	N/A	200	ms	V_{DD} maximum ramp time from 300mV to V_{DD} minimum
V_{DDQ}_ona	N/A	200	ms	V_{DDQ} maximum ramp time from 300mV to V_{DDQ} minimum

Notes: 1. 20 MHz band-limited measurement.

   - Condition A:
     - Apply V_{PP} without any slope reversal before or at the same time as V_{DD} and V_{DDQ}.
     - V_{DD} and V_{DDQ} are driven from a single-power converter output and apply V_{DD}/V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
     - The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
     - V_{TT} is limited to 0.76V MAX when the power ramp is complete.
     - V_{REFCA} tracks V_{DD}/2.

– Condition B:
  - Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
  - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
  - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
  - The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

2. After RESET_n is de-asserted, wait for a minimum of 500µs, but no longer than 3 seconds, before allowing CKE to be registered HIGH at clock edge Td. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^{t}CK (whichever is larger) before CKE is registered HIGH at clock edge Td. Because CKE is a synchronous signal, the corresponding setup time to clock (^{t}IS) must be met. Also, a DESELECT command must be registered (with ^{t}IS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^{t}DLLK and ^{t}ZQinit.
4. The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until ^{t}IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^{t}DLLK and ^{t}ZQinit.
5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ^{t}XPR, before issuing the first MRS command to load mode register (^{t}XPR = MAX (^{t}XS, 5 × ^{t}CK).
6. Issue MRS command to load MR3 with all application settings, wait ^{t}MRD.
7. Issue MRS command to load MR6 with all application settings, wait ^{t}MRD.
8. Issue MRS command to load MR5 with all application settings, wait ^{t}MRD.
9. Issue MRS command to load MR4 with all application settings, wait ^{t}MRD.
10. Issue MRS command to load MR2 with all application settings, wait ^{t}MRD.
11. Issue MRS command to load MR1 with all application settings, wait ^{t}MRD.
12. Issue MRS command to load MR0 with all application settings, wait ^{t}MOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for ^{t}DLLK and ^{t}ZQinit to complete.
15. The device will be ready for normal operation. Once the DRAM has been initialized, if the DRAM is in an idle state longer than 960ms, then either (a) REF commands must be issued within ^{t}REFI constraints (specification for posting allowed) or (b) CKE or CS_n must toggle once within every 960ms interval of idle time. For debug purposes, the 960ms delay limit maybe extended to 60 minutes provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.
16. Optional MBIST-PPR mode can be entered by setting MR4:A0 to 1, followed by subsequent MR0 guard key sequences, then DRAM will drive ALERT_n to LOW. DRAM will drive ALERT_n to HIGH

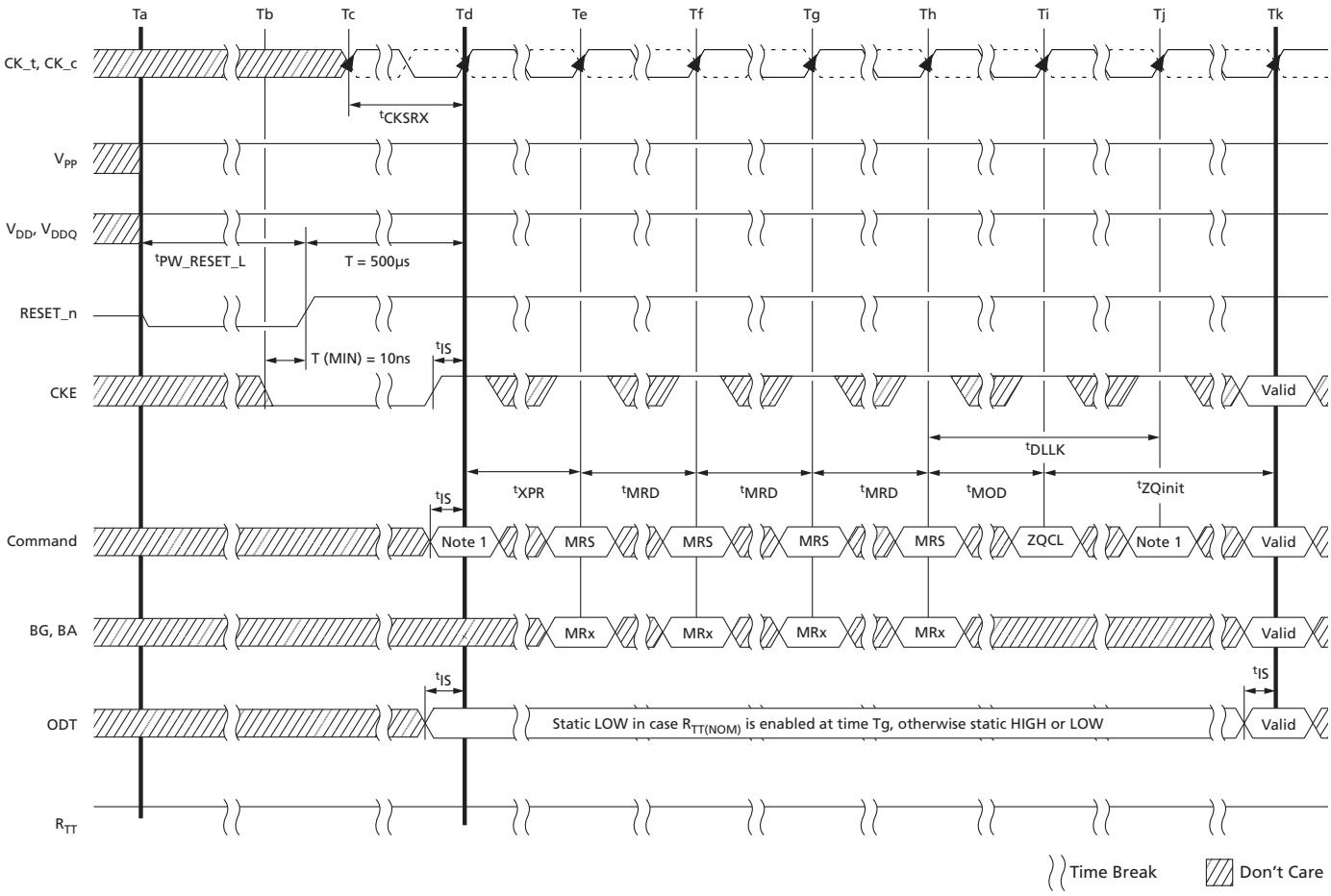
to indicate that this operation is completed. MBIST-PPR mode can take place anytime after Tk. Note that no exit sequence or re-initialization is needed after MBIST completes; As soon as ALERT_N goes HIGH and ^{t}IS is satisfied, MR0 must be re-written to the pre guard key state, then and the DRAM is immediately ready to receive valid commands.

A stable valid V_{DD} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DD} provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.

A stable valid V_{DDQ} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.

A stable valid V_{PP} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±120mV (greater than 250 KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.

Figure 15: RESET and Initialization Sequence at Power-On Ramping



Notes: 1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.
5. Optional MBIST-PPR may be entered any time after Tk.

RESET Initialization with Stable Power Sequence

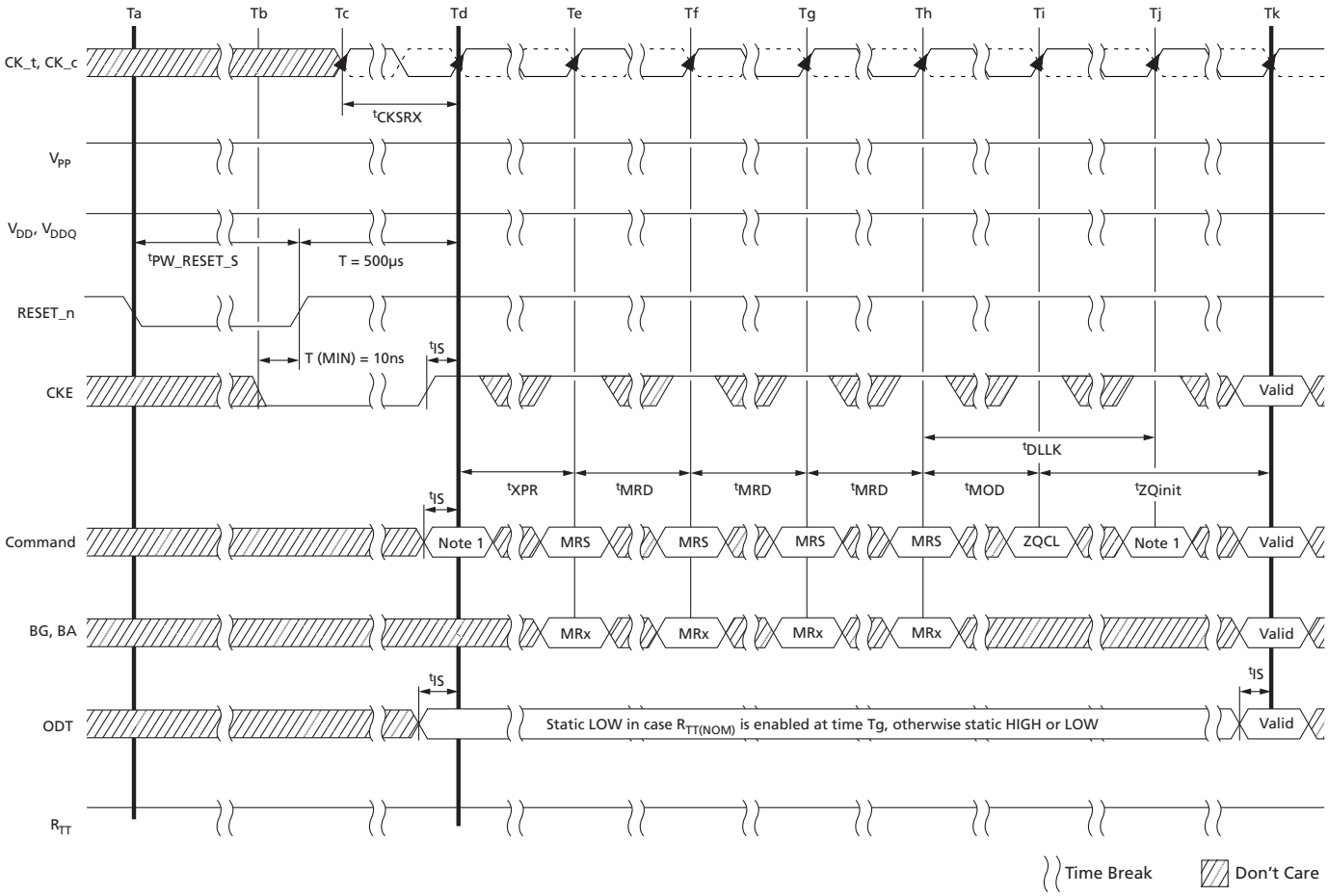
The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET_n below 0.2 × V_{DD} any time when reset is needed (all other inputs may be undefined).

   RESET_n needs to be maintained for minimum ^{t}PW_RESET. CKE is pulled LOW before RESET_n being de-asserted (minimum time 10ns).
2. Follow Steps 2 through 10 in the Reset and Initialization Sequence at Power-On Ramping procedure.

When the reset sequence is complete, all counters except the refresh counters have been reset and the device is ready for normal operation.

Figure 16: RESET Procedure at Power Stable Condition



Notes: 1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.

3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.

Uncontrolled Power-Down Sequence

In the event of an uncontrolled ramping down of V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- Condition B: The amount that V_{PP} may be less than V_{DD}/V_{DDQ} is less than or equal to 500mV.
- Condition C: The time V_{PP} may be less than V_{DD} is ≤10ms per occurrence with a total accumulated time in this state ≤100ms.
- Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is ≤15ms per occurrence with a total accumulated time in this state ≤150ms.

Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MR*n*) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

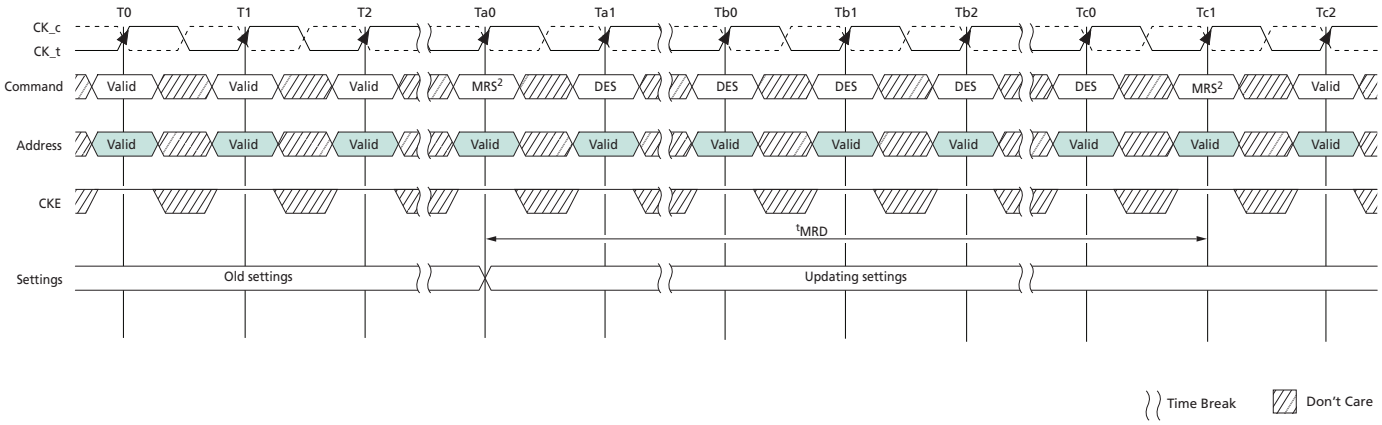
The MRS command cycle time, ^{t}MRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the ^{t}MRD Timing figure.

Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply ^{t}MRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- CMD address latency
- CA parity latency mode
- V_{REFDQ} training value
- V_{REFDQ} training mode
- V_{REFDQ} training range

Some mode register settings may not be supported because they are not required by certain speed bins.

Figure 17: tMRD Timing

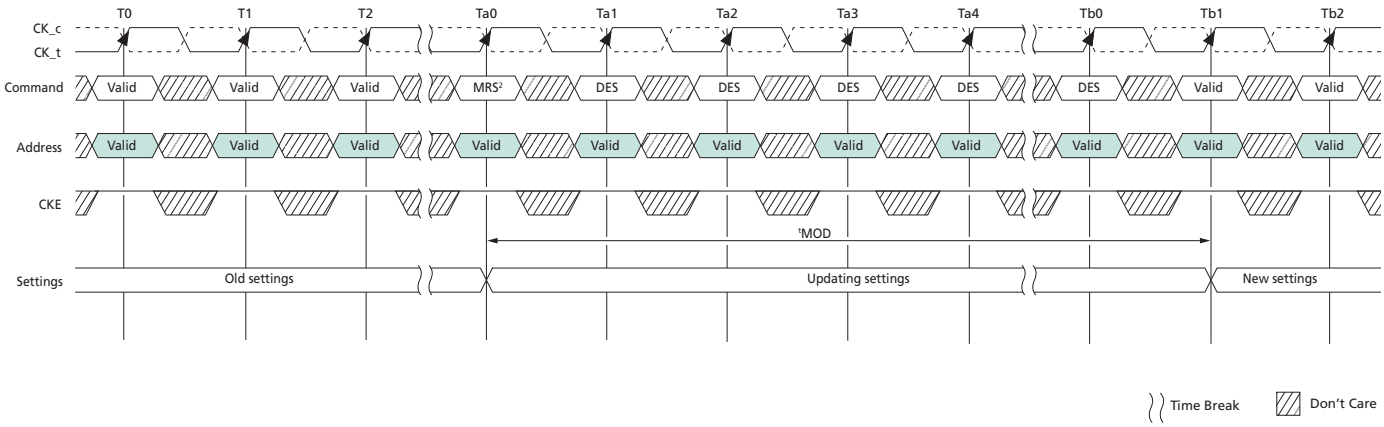


Notes: 1. This timing diagram depicts CA parity mode "disabled" case.

2. tMRD applies to all MRS commands with the following exceptions:
   Gear-down mode
   CA parity latency mode
   CMD address latency
   Per-DRAM addressability mode
   V_{REFDQ} training value, V_{REFDQ} training mode, and V_{REFDQ} training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except for those noted in note 2 in figure below where the individual function descriptions may specify a different requirement. tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the tMOD Timing figure.

Figure 18: tMOD Timing



Notes: 1. This timing diagram depicts CA parity mode "disabled" case.

2. tMOD applies to all MRS commands with the following exceptions:
   DLL enable, DLL RESET, Gear-down mode
   V_{REFDQ} training value, internal V_{REF} training monitor, V_{REFDQ} training mode, and V_{REFDQ} training range
   Maximum power savings mode, Per-DRAM addressability mode, and CA parity latency mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If

the $R_{TT(NOM)}$ feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring R_{TT} is in an off state prior to the MRS command.

The ODT signal may be registered HIGH after ^{t}MOD has expired. If the $R_{TT(NOM)}$ feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes.

In some mode register setting cases, function updating takes longer than ^{t}MOD. This type of MRS does not apply ^{t}MOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

Mode Register 0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 6: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 7: MR0 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** **000 = MR0** 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13,11:9	**WR (WRITE recovery)/RTP (READ-to-PRECHARGE)** 0000 = 10 / 5 clocks[1] 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks[1] 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks[1] 0101 = 20 /10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks[1] 1000 = 26 / 13 clocks[1] 1001 = 28 / 14 clocks[2] 1010 through 1111 = Reserved
8	**DLL reset** 0 = No 1 = Yes

Table 7: MR0 Register Definition (Continued)

Mode Register	Description
7	**Test mode (TM) – Manufacturer use only** 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	**CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out** 00000 = 9 clocks[1] 00001 = 10 clocks 00010 = 11 clocks[1] 00011 = 12 clocks 00100 = 13 clocks[1] 00101 = 14 clocks 00110 = 15 clocks[1] 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks[1] 01101 = 17 clocks[1] 01110 = 19 clocks[1] 01111 = 21 clocks [1] 10000 = 25 clocks 10001 = 26 clocks 10011 = 28 clocks 10100 = 29 clocks[1] 10101 = 30 clocks 10110 = 31 clocks[1] 10111 = 32 clocks
3	**Burst type (BT) – Data burst ordering within a READ or WRITE burst access** 0 = Nibble sequential 1 = Interleave
1:0	**Burst length (BL) – Data burst size associated with each read or write access** 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.
2. If WR requirement exceeds 28 clocks or RTP exceeds 14 clocks, WR should be set to 28 clocks and RTP should be set to 14 clocks.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 8: Burst Type and Burst Order

Note 1 applies to the entire table

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

Notes: 1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for ^{t}WR and ^{t}WTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for ^{t}WR and ^{t}WTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
3. T = Output driver for data and strobes are in High-Z.
V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X = "Don't Care."

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery (WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with ^{t}RP to determine ^{t}DAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section. The WR value must be programmed to be equal to or larger than ^{t}WR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; ^{t}WR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data.

Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing ^{t}RTP (in ns) by ^{t}CK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section. The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with ^{t}RP to determine the ACT timing to the same bank.

DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, ^{t}DLLK must be met before functions requiring the DLL can be used. Such as READ commands or synchronous ODT operations, for example.

Mode Register 1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 9: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 10: MR1 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 **001 = MR1** 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) 1 = Disabled (both ODI and R_{TT})
11	**Termination data strobe (TDQS) – Additional termination pins (x8 configuration only)** 0 = TDQS disabled 1 = TDQS enabled
10, 9, 8	**Nominal ODT ($R_{TT(NOM)}$) – Data bus termination setting** 000 = $R_{TT(NOM)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)

Table 10: MR1 Register Definition (Continued)

Mode Register	Description
7	**Write leveling (WL) – Write leveling mode** 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
13, 6, 5	**Rx CTLE Control** 000 = Vendor Default 001 = Vendor Defined 010 = Vendor Defined 011 = Vendor Defined 100 = Vendor Defined 101 = Vendor Defined 110 = Vendor Defined 111 = Vendor Defined
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 1[1] 10 = CL - 2 11 = Reserved
2, 1	**Output driver impedance (ODI) – Output driver impedance setting** 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, ^{t}DLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}DQSCK, ^{t}AON, or ^{t}AOF parameters.

During ^{t}DLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when $R_{TT(WR)}$ is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the $R_{TT(NOM)}$ bits MR1[9,6,2] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set $R_{TT(WR)}$, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT $R_{TT(NOM)}$ Values

The device is capable of providing three different termination values: $R_{TT(Park)}$, $R_{TT(NOM)}$, and $R_{TT(WR)}$. The nominal termination value, $R_{TT(NOM)}$, is programmed in MR1. A separate value, $R_{TT(WR)}$, may be programmed in MR2 to enable a unique R_{TT} value when ODT is enabled during WRITE operations. The $R_{TT(WR)}$ value can be applied during WRITE commands even when $R_{TT(NOM)}$ is disabled. A third R_{TT} value, $R_{TT(Park)}$, is programed in MR5. $R_{TT(Park)}$ provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 11: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Notes: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Rx CTLE Control

The Mode Register for Rx CTLE Control MR1[A13,A6,A5] is vendor specific. Since CTLE circuits can not be typically bypassed a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected

from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

Termination Data Strobe

Termination data strobe (TDQS) is a feature of the x8 device and provides additional termination resistance outputs that may be useful in some system configurations. Because this function is available only in a x8 configuration, it must be disabled for x4 and x16 configurations.

While TDQS is not supported in x4 or x16 configurations, the same termination resistance function that is applied to the TDQS pins is applied to the DQS pins when enabled via the mode register.

The TDQS, DBI, and DATA MASK (DM) functions share the same pin. When the TDQS function is enabled via the mode register, the DM and DBI functions are not supported. When the TDQS function is disabled, the DM and DBI functions can be enabled separately.

Table 12: TDQS Function Matrix

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	**Enabled**	Disabled	**Enabled** or disabled
	Disabled	**Enabled**	**Enabled** or disabled
	Disabled	Disabled	**Enabled** or disabled
Enabled	Disabled	Disabled	Disabled

Mode Register 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 13: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 14: MR2 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 **010 = MR2** 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**WRITE data bus CRC** 0 = Disabled 1 = Enabled
11:9	**Dynamic ODT ($R_{TT(WR)}$) – Data bus termination setting during WRITEs** 000 = $R_{TT(WR)}$ disabled (WRITE does not affect R_{TT} value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved

Table 14: MR2 Register Definition (Continued)

Mode Register	Description
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (T_C: -40°C–85°C) 01 = Manual mode - Reduced operating temperature range (T_C: -40°C–45°C) 10 = Manual mode - Extended operating temperature range (T_C: -40°C–105°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1^{t}CK WRITE preamble** 000 = 9 (DDR4-1600)[1] 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600)[1] 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2^{t}CK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	**RFU** 0 = Must be programmed to 0 1 = Reserved
1:0	**RFU** 0 = Must be programmed to 0 1 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the I_{DD6} current for a given temperature range as specified in the MR2 Register Definition table.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT ($R_{TT(WR)}$) settings in MR2[11:9]. In write leveling mode, only $R_{TT(NOM)}$ is available.

Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

Mode Register 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 15: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 16: MR3 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 **011 = MR3** 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:11	**Multipurpose register (MPR) – Read format** 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	**WRITE CMD latency when CRC/DM enabled** 00 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400/2666) 10 = 6CK (DDR4-2933/3200) 11 = Reserved

Table 16: MR3 Register Definition (Continued)

Mode Register	Description
8:6	**Fine granularity refresh mode** 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	**Temperature sensor status** 0 = Disabled 1 = Enabled
4	**Per-DRAM addressability** 0 = Normal operation (disabled) 1 = Enable
3	**Gear-down mode – Ratio of internal clock to external data rate** 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	**Multipurpose register (MPR) access** 0 = Normal operation 1 = Data flow from MPR
1:0	**MPR page select** 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MR*n* registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and ^{t}RP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4nCK is used, 5nCK or 6nCK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666

MT/s then 5nCK is used, 4nCK or 6nCK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6nCK is used; 4nCK or 5nCK are not allowed.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening ^{t}RFC and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or V_{REF} values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

Mode Register 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 17: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET (MRS) command.

Table 18: MR4 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 **100 = MR4** 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**Hard Post Package Repair (hPPR mode)** 0 = Disabled 1 = Enabled
12	**WRITE preamble setting** 0 = 1^{t}CK toggle[1] 1 = 2^{t}CK toggle (When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.)
11	**READ preamble setting** 0 = 1^{t}CK toggle[1] 1 = 2^{t}CK toggle
10	**READ preamble training** 0 = Disabled 1 = Enabled

Table 18: MR4 Register Definition (Continued)

Mode Register	Description
9	**Self refresh abort mode** 0 = Disabled 1 = Enabled
8:6	**CMD (CAL) address latency** 000 = 0 clocks (disabled) 001 =3 clocks[1] 010 = 4 clocks 011 = 5 clocks[1] 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	**soft Post Package Repair (sPPR mode)** 0 = Disabled 1 = Enabled
4	**Internal V_{REF} monitor** 0 = Disabled 1 = Enabled
3	**Temperature controlled refresh mode** 0 = Disabled 1 = Enabled
2	**Temperature controlled refresh range** 0 = Normal temperature mode 1 = Extended temperature mode
1	**Maximum power savings mode** 0 = Normal operation 1 = Enabled
0	**MBIST-PPR** 0 = Disabled 1 = Enabled

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Hard Post Package Repair Mode

The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether hPPR mode is available (A7 = 1) or not available (A7 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

WRITE Preamble

Programmable WRITE preamble, ^{t}WPRE, can be set to 1^{t}CK or 2^{t}CK via the MR4 register. The 1^{t}CK setting is similar to DDR3. However, when operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble

Programmable READ preamble ^{t}RPRE can be set to 1^{t}CK or 2^{t}CK via the MR4 register. Both the 1^{t}CK and 2^{t}CK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

READ Preamble Training

Programmable READ preamble training can be set to 1^{t}CK or 2^{t}CK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of -40°C to 85°C, while the extended temperature range covers -40°C to 105°C.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register according to the ^{t}CAL(ns)/^{t}CK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Internal V_{REF} Monitor

This mode enables output of internally generated V_{REFDQ} for monitoring on DQ0, DQ1, DQ2, and DQ3. May be used during V_{REFDQ} training and test. While in this mode, R_{TT} should be set to High-Z. V_{REF_time} must be increased by 10ns if DQ load is 0pF, plus an additional 15ns per pF of loading. This measurement is for verification purposes and is NOT an external voltage supply pin.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

MBIST-PPR

This mode is JEDEC optional and allows for a self-contained DRAM test and repair. Please refer to the Features list on page 1 for a list of die revisions that support MBIST-PPR.

Mode Register 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 19: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 20: MR5 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 **101 = MR5** 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled 1 = Enabled
10	**Data mask (DM)** 0 = Disabled 1 = Enabled
9	**CA parity persistent error mode** 0 = Disabled 1 = Enabled

Table 20: MR5 Register Definition (Continued)

Mode Register	Description
8:6	**Parked ODT value ($R_{TT(Park)}$)** 000 = $R_{TT(Park)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	**ODT input buffer for power-down** 0 = Buffer enabled 1 = Buffer disabled
4	**CA parity error status** 0 = Clear 1 = Error
3	**CRC error status** 0 = Clear 1 = Error
2:0	**CA parity latency mode** 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400/2666)[1] 011 = 6 clocks (DDR4-2933/3200) 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

DBI is not supported for 3DS devices and should be disabled in MR5.

Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. However, the device may provide $R_{TT(Park)}$ termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on ^{t}CK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

Mode Register 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 21: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 22: MR6 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 **110 = MR6** 111 = DNU
17	**NA on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
12:10	**Data rate** 000 = Data rate≤ 1333 Mb/s (1333 Mb/s) 001 = 1333 Mb/s < Data rate ≤ 1866 Mb/s (1600, 1866 Mb/s) 010 = 1866 Mb/s < Data rate ≤ 2400 Mb/s (2133, 2400 Mb/s) 011 = 2400 Mb/s < Data rate ≤ 2666 Mb/s (2666 Mb/s) 100 = 2666 Mb/s < Data rate ≤ 3200 Mb/s (2933, 3200 Mb/s) 101 = Reserved 110 = Reserved 111 = Reserved

Table 22: MR6 Register Definition (Continued)

Mode Register	Description
13, 9, 8	**RFU** Default = 000; Must be programmed to 000 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved
7	**V_{REF} Calibration Enable** 0 = Disable 1 = Enable
6	**V_{REF} Calibration Range** 0 = Range 1 1 = Range 2
5:0	**V_{REF} Calibration Value** See the V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section

Data Rate Programming

The device controller must program the correct data rate according to the operating frequency.

V_{REFDQ} Calibration Enable

V_{REFDQ} calibration is where the device internally generates its own V_{REFDQ} to be used by the DQ input receivers. The V_{REFDQ} value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal V_{REFDQ} level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conjunction with V_{REFDQ} adjustments to optimize and verify the data eye. Enabling V_{REFDQ} calibration must be used whenever values are being written to the MR6[6:0] register.

V_{REFDQ} Calibration Range

The device defines two V_{REFDQ} calibration ranges: Range 1 and Range 2. Range 1 supports V_{REFDQ} between 60% and 92% of V_{DDQ} while Range 2 supports V_{REFDQ} between 45% and 77% of V_{DDQ}, as seen in V_{REFDQ} Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

V_{REFDQ} Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V_{REFDQ}, as seen in V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section.

Truth Tables

Table 23: Truth Table – Command

Notes 1–5 apply to the entire table; Note 6 applies to all READ/WRITE commands

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
MODE REGISTER SET		MRS	H	H	L	H	L	L	L	BG	BA	V	OP code				7
REFRESH		REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	8, 9, 10
Self refresh exit		SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	8, 9, 10, 11
					L	H	H	H	H	V	V	V	V	V	V	V	
Single-bank PRECHARGE		PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
Reserved for future use		RFU	H	H	L	H	L	H	H	RFU							
Bank ACTIVATE		ACT	H	H	L	L	Row address (RA)			BG	BA	V	Row address (RA)				
WRITE	BL8 fixed, BC4 fixed	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
	BC4OTF	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
	BL8OTF	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
WRITE with auto pre-charge	BL8 fixed, BC4 fixed	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
	BC4OTF	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
	BL8OTF	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
READ	BL8 fixed, BC4 fixed	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
	BC4OTF	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
	BL8OTF	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	

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Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
READ with auto pre-charge	BL8 fixed, BC4 fixed	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
	BC4OTF	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
	BL8OTF	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
NO OPERATION		NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	12
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	13
Power-down entry		PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
Power-down exit		PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	H	L	X	X	X	X	X	H	X	
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	H	L	X	X	X	X	X	L	X	

- BG = Bank group address
- BA = Bank address
- RA = Row address
- CA = Column address
- BC_n = Burst chop
- X = "Don't Care"
- V = Valid

2. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT_n = H, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n, respectively. When ACT_n = L, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14, respectively.
3. RESET_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
4. Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
5. V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
6. READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
7. During an MRS command, A17 is RFU and is device density- and configuration-dependent.
8. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
9. V_{PP} and V_{REF} (V_{REFCA}) must be maintained during SELF REFRESH operation.
10. Refer to the Truth Table – CKE table for more details about CKE transition.
11. Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
12. The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.

13. The NOP command may not be used in place of the DESELECT command.
14. The power-down mode does not perform any REFRESH operation.

Table 24: Truth Table – CKE

Notes 1–7, 9, and 20 apply to the entire table

Current State	CKE		Command (n)	Action (n)	Notes
	Previous Cycle (n - 1)	Present Cycle (n)			
Power-down	L	L	X	Maintain power-down	8, 10, 11
	L	H	DES	Power-down exit	8, 10, 12
Self refresh	L	L	X	Maintain self refresh	11, 13
	L	H	DES	Self refresh exit	8, 13, 14, 15
Bank(s) active	H	L	DES	Active power-down entry	8, 10, 12, 16
Reading	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Writing	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Precharging	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Refreshing	H	L	DES	Precharge power-down entry	8, 12
All banks idle	H	L	DES	Precharge power-down entry	8, 10, 12, 16, 18
	H	L	REFRESH	Self refresh	16, 18, 19

Notes:
1. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
2. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
3. COMMAND (n) is the command registered at clock edge n, and ACTION (n) is a result of COMMAND (n); ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
6. During any CKE transition (registration of CKE H->L or CKE H->L), the CKE level must be maintained until 1 nCK prior to ^{t}CKE (MIN) being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Truth Table – Command table.
8. For power-down entry and exit parameters, see the Power-Down Modes section.
9. CKE LOW is allowed only if ^{t}MRD and ^{t}MOD are satisfied.
10. The power-down mode does not perform any REFRESH operations.
11. X = "Don't Care" (including floating around V_{REF}) in self refresh and power-down. X also applies to address pins.
12. The DESELECT command is the only valid command for power-down entry and exit.
13. V_{PP} and V_{REFCA} must be maintained during SELF REFRESH operation.
14. On self refresh exit, the DESELECT command must be issued on every clock edge occurring during the ^{t}XS period. READ or ODT commands may be issued only after ^{t}XSDLL is satisfied.
15. The DESELECT command is the only valid command for self refresh exit.
16. Self refresh cannot be entered during READ or WRITE operations. For a detailed list of restrictions see the SELF REFRESH Operation and Power-Down Modes sections.
17. If all banks are closed at the conclusion of the READ, WRITE, or PRECHARGE command, then precharge power-down is entered; otherwise, active power-down is entered.

18. Idle state is defined as all banks are closed (^{t}RP, ^{t}DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (^{t}MRD, ^{t}MOD, ^{t}RFC, ^{t}ZQinit, ^{t}ZQoper, ^{t}ZQCS, and so on), as well as all self refresh exit and power-down exit parameters are satisfied (^{t}XS, ^{t}XP, ^{t}XSDLL, and so on).
19. Self refresh mode can be entered only from the all banks idle state.
20. For more details about all signals, see the Truth Table – Command table; must be a legal command as defined in the table.

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP (CS_n = LOW and ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. NOP command general support has been removed and the command should not be used unless specifically allowed, which is when exiting maximum power-saving mode or when entering gear-down mode.

DESELECT Command

The deselect function (CS_n HIGH) prevents new commands from being executed; therefore, with this command, the device is effectively deselected. Operations already in progress are not affected.

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0, which will disable the DLL for subsequent operations until the A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off mode is specified by the parameter ^{t}CKDLL_OFF.

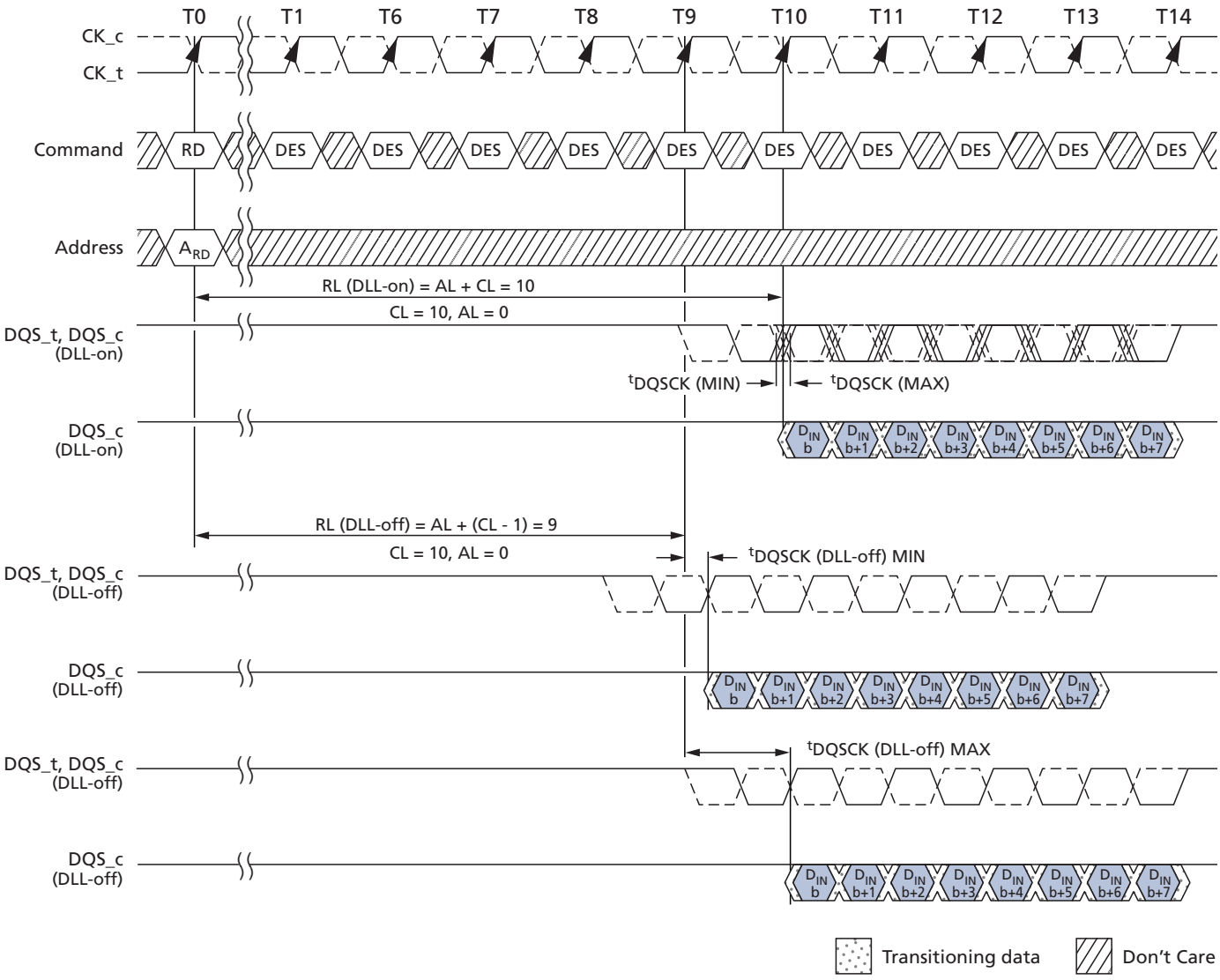
Due to latency counter and timing restrictions, only one CL value and CWL value (in MR0 and MR2 respectively) are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

DLL-off mode will affect the read data clock-to-data strobe relationship (^{t}DQSCK), but not the data strobe-to-data relationship (^{t}DQSQ,^{t}QH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where ^{t}DQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode ^{t}DQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that ^{t}DQSCK may not be small compared to^{t}CK (it might even be larger than ^{t}CK), and the difference between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX) is significantly larger than in DLL-on mode. The ^{t}DQSCK (DLL-off) values are undefined and the user is responsible for training to the data-eye.

The timing relations on DLL-off mode READ operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.

Figure 19: DLL-Off Mode Read Timing Operation



DLL-On/Off Switching Procedures

The DLL-off mode is entered by setting MR1 bit A0 to 0; this will disable the DLL for subsequent operations until the A0 bit is set back to 1.

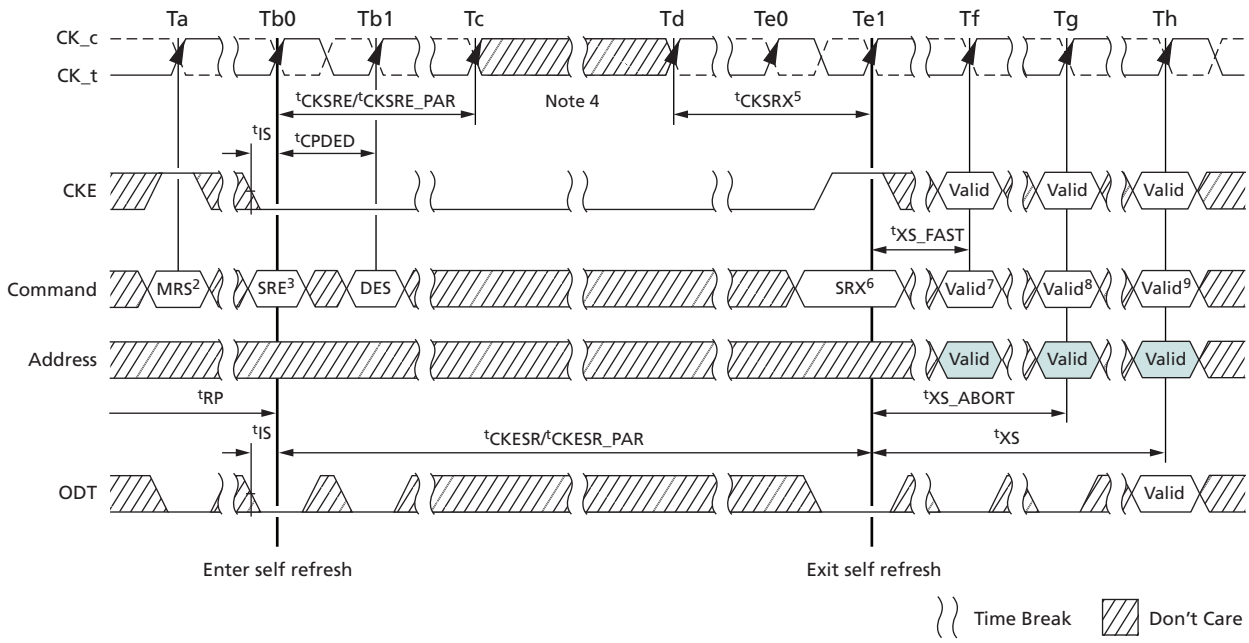
DLL Switch Sequence from DLL-On to DLL-Off

To switch from DLL-on to DLL-off requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and, to disable the DLL, the DRAM on-die termination resistors, $R_{TT(NOM)}$, must be in High-Z before MRS to MR1.)
2. Set MR1 bit A0 to 1 to disable the DLL.
3. Wait ^{t}MOD.
4. Enter self refresh mode; wait until ^{t}CKSRE/^{t}CKSRE_PAR is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least ^{t}CKSRX at device inputs.
7. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until all ^{t}MOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all ^{t}MOD timings from any MRS command are satisfied. If $R_{TT(NOM)}$ was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait ^{t}XS_FAST, ^{t}XS_ABORT, or ^{t}XS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after ^{t}XS_FAST).
   - ^{t}XS_FAST: ZQCL, ZQCS, and MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and gear-down mode in MR3 may be accessed provided the device is not in per-DRAM addressability mode. Access to other device mode registers must satisfy ^{t}XS timing.
   - ^{t}XS_ABORT: If MR4 [9] is enabled, then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of ^{t}XS_ABORT. Upon exiting from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same regardless of the MRS bit setting for self refresh abort.
   - ^{t}XS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, and RDAS8.
9. Wait ^{t}MOD to complete.

The device is ready for the next command.

Figure 20: DLL Switch Sequence from DLL-On to DLL-Off



Notes: 1. Starting in the idle state. R_{TT} in stable state.
2. Disable DLL by setting MR1 bit A0 to 0.
3. Enter SR.
4. Change frequency.
5. Clock must be stable ^{t}CKSRX.
6. Exit SR.
7. Update mode registers allowed with DLL-off settings met.

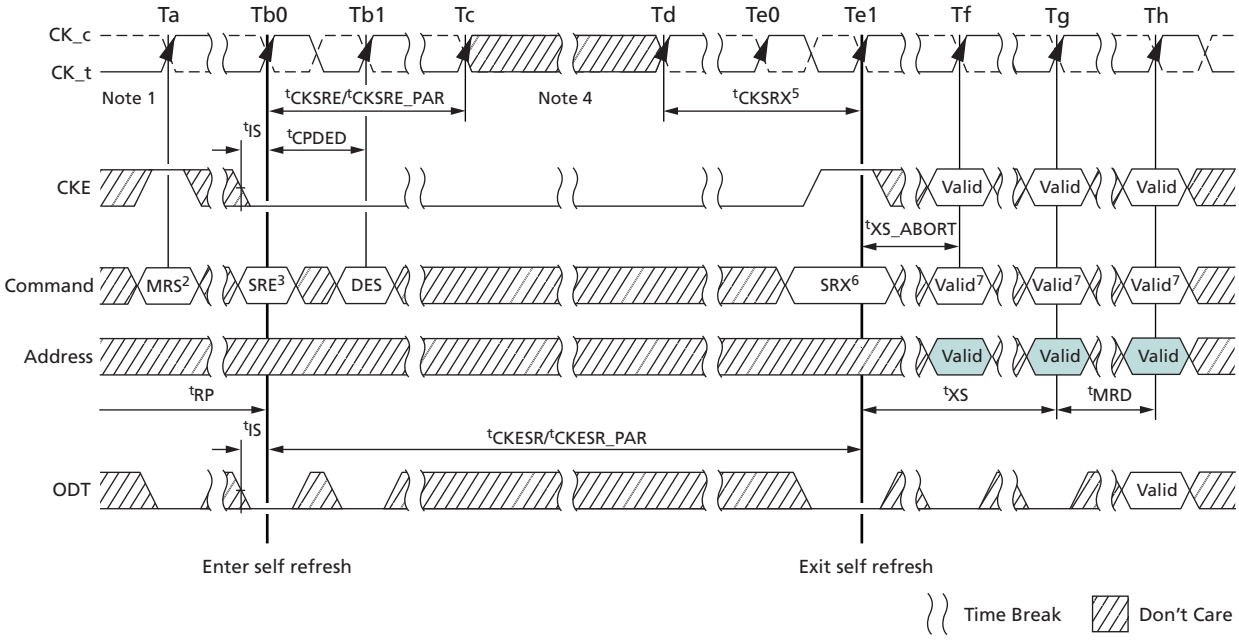
DLL-Off to DLL-On Procedure

To switch from DLL-off to DLL-on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM ODT resistors ($R_{TT(NOM)}$) must be in High-Z before self refresh mode is entered.)
2. Enter self refresh mode; wait until ^{t}CKSRE/^{t}CKSRE_PAR are satisfied.
3. Change frequency (following the guidelines in the Input Clock Frequency Change section).
4. Wait until a stable clock is available for at least ^{t}CKSRX at device inputs.
5. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW or HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. If $R_{TT(NOM)}$ disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait ^{t}XS or ^{t}XS_ABORT, depending on bit 9 in MR4, then set MR1 bit A0 to 0 to enable the DLL.
7. Wait ^{t}MRD, then set MR0 bit A8 to 1 to start DLL reset.
8. Wait ^{t}MRD, then set mode registers with appropriate values; an update of CL, CWL, and WR may be necessary. After ^{t}MOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after ^{t}DLLK.
9. Wait for ^{t}MOD to complete. Remember to wait ^{t}DLLK after DLL RESET before applying any command requiring a locked DLL. In addition, wait for ^{t}ZQoper in case a ZQCL command was issued.

The device is ready for the next command.

Figure 21: DLL Switch Sequence from DLL-Off to DLL-On



Notes: 1. Starting in the idle state.
2. Enter SR.
3. Change frequency.

4. Clock must be stable ^{t}CKSRX.
5. Exit SR.
6. Set DLL to on by setting MR1 to A0 = 0.
7. Update mode registers.
8. Issue any valid command.

Input Clock Frequency Change

After the device is initialized, it requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

After the device has been successfully placed in self refresh mode and ^{t}CKSRE/^{t}CKSRE_PAR have been satisfied, the state of the clock becomes a "Don't Care." Following a "Don't Care," changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in SELF REFRESH Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, gear-down mode, READ and WRITE preamble, Command Address Latency, and data rate values.

When the clock rate is being increased (faster), the MR settings that require additional clocks should be updated prior to the clock rate being increased. In particular, the PL latency must be disabled when the clock rate changes, ie. while in self refresh mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA parity mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. The correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter self refresh mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit self refresh mode, (5) Enable CA parity mode setting PL = 6 vis MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, for example. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the IDLE state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to the next time the DRAM enters the IDLE state.

If MR6 is issued prior to self refresh entry for the new data rate value, DLL will relock automatically at self refresh exit. However, if MR6 is issued after self refresh entry, MR0 must be issued to reset the DLL.

The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence (see DLL-On/Off Switching Procedures).

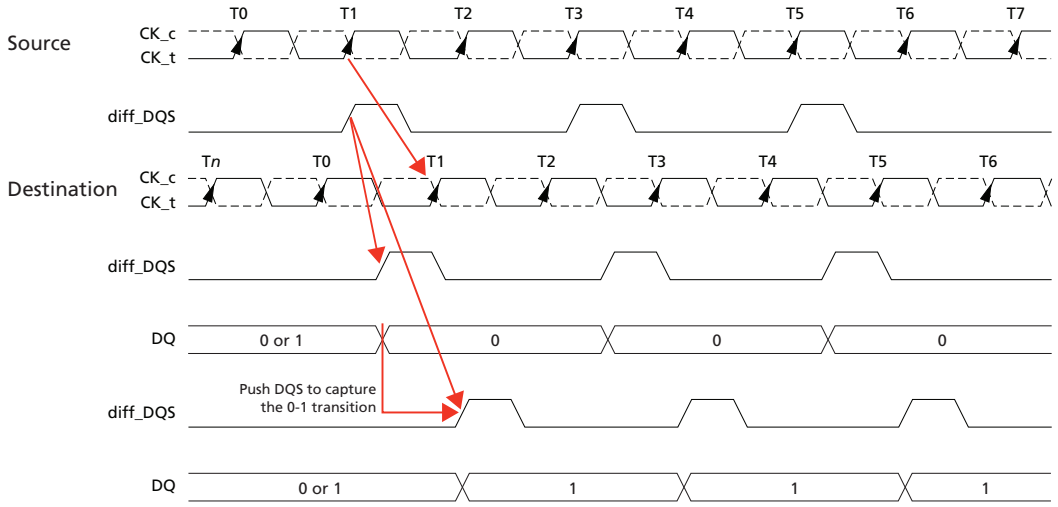
Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS,^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature

may not be required under some system conditions, provided the host can maintain the ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the ^{t}DQSS specification. Besides ^{t}DQSS, ^{t}DSS and ^{t}DSH specifications also need to be fulfilled. One way to achieve this is to combine the actual ^{t}DQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual ^{t}DQSS in the application, the actual values for ^{t}DQSL and ^{t}DQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy ^{t}DSS and ^{t}DSH specifications. A conceptual timing of this scheme is shown below.

Figure 22: Write Leveling Concept, Example 1

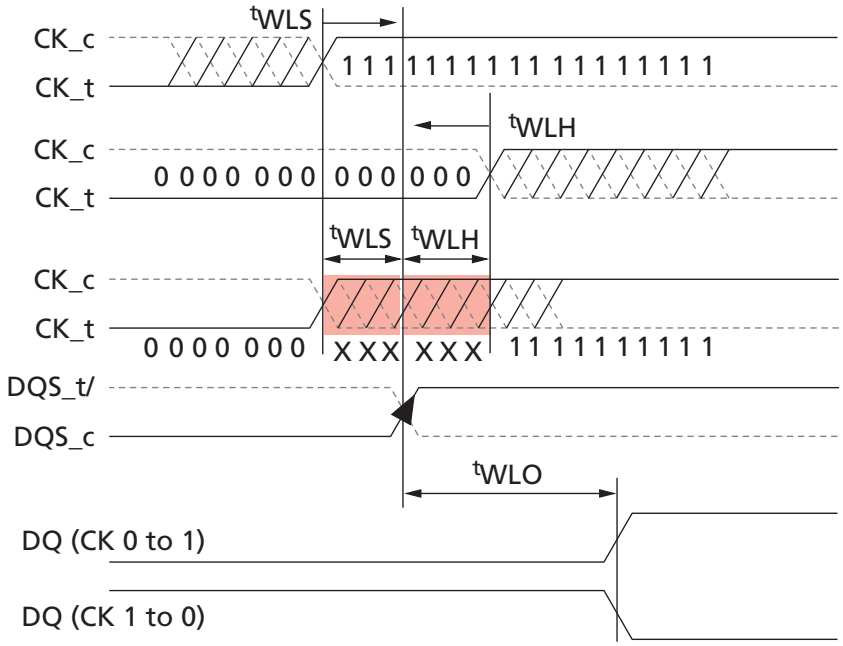


DQS driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations: x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS(diff_LDQS)-to-clock relationship.

The figure below is another representative way to view the write leveling procedure. Although it shows the clock varying to a static strobe, this is for illustrative purpose only; the clock does not actually change phase, the strobe is what actually varies. By issuing multiple WL bursts, the DQS strobe can be varied to capture with fair accuracy the time at which the clock edge arrives at the DRAM clock input buffer.

Figure 23: Write Leveling Concept, Example 2



DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode

The DRAM enters into write leveling mode if A7 in MR1 is HIGH. When leveling is finished, the DRAM exits write leveling mode if A7 in MR1 is LOW (see the MR Leveling Procedures table). Note that in write leveling mode, only DQS terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM DRAM TERMINATION Function in Leveling Mode table).

Table 25: MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Q off)	A12	0	1

Table 26: DRAM TERMINATION Function in Leveling Mode

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination
$R_{TT(NOM)}$ with ODT HIGH	On	Off
$R_{TT(Park)}$ with ODT LOW	On	Off

Notes: 1. In write leveling mode, with the mode's output buffer either disabled (MR1[bit7] = 1 and MR1[bit12] = 1) or with its output buffer enabled (MR1[bit7] = 1 and MR1[bit12] = 0), all $R_{TT(NOM)}$ and $R_{TT(Park)}$ settings are supported.
2. $R_{TT(WR)}$ is not allowed in write leveling mode and must be set to disable prior to entering write leveling mode.

Procedure Description

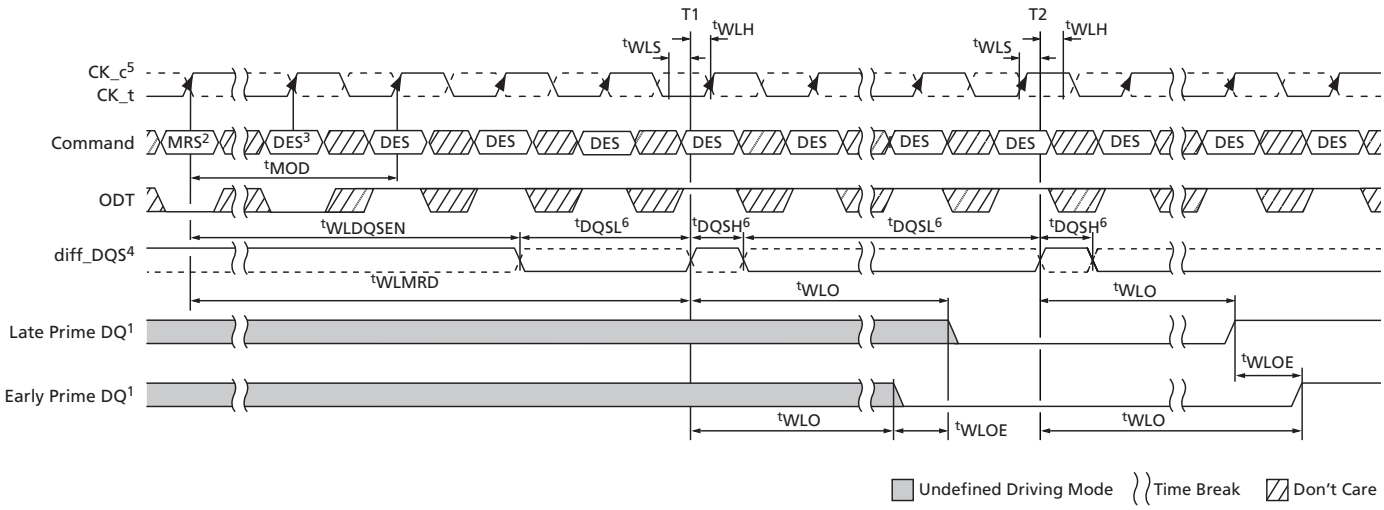
The memory controller initiates the leveling mode of all DRAM by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT command is supported, other than MRS commands to change the Qoff bit (MR1[A12]) and to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change the other MR1 bits. Because the controller levels

one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal, unless DODTLon or DODTLoff have been altered (the ODT internal pipe delay is increased when increasing WRITE latency [WL] or READ latency [RL] by the previous MR command), then ODT assertion should be delayed by DODTLon after tMOD is satisfied, which means the delay is now tMOD + DODTLon.

The controller may drive DQS_t LOW and DQS_c HIGH after a delay of tWLDQSEN, at which time the DRAM has applied ODT to these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge, which is used by the DRAM to sample CK driven from the controller. tWLMRD (MAX) timing is controller dependent.

The DRAM samples CK status with the rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t, DQS_c) needed for these DQs. The controller samples incoming DQ and either increments or decrements DQS delay setting and launches the next DQS pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.

Figure 24: Write Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2)



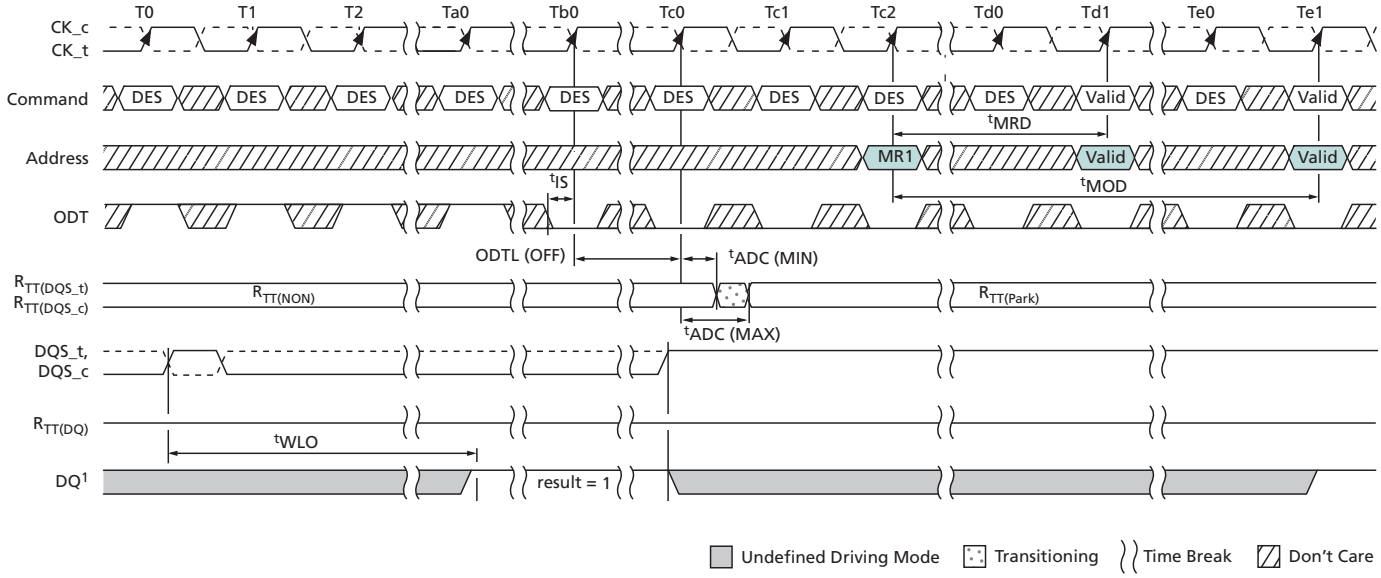
Notes: 1. The device drives leveling feedback on all DQs.
2. MRS: Load MR1 to enter write leveling mode.
3. diff_DQS is the differential data strobe. Timing reference points are the zero crossings. DQS_t is shown with a solid line; DQS_c is shown with a dotted line.
4. CK_t is shown with a solid dark line; CK_c is shown with a dotted line.
5. DQS needs to fulfill minimum pulse width requirements, tDQSH (MIN) and tDQSL (MIN), as defined for regular WRITEs; the maximum pulse width is system dependent.
6. tWLDQSEN must be satisfied following equation when using ODT:
   - DLL = Enable, then tWLDQSEN > tMOD (MIN) + DODTLon + tADC
   - DLL = Disable, then tWLDQSEN > tMOD (MIN) + tAONAS

Write Leveling Mode Exit

Write leveling mode should be exited as follows:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until ^{t}MOD after the respective MR command (Te1).
2. Drive ODT pin LOW (^{t}IS must be satisfied) and continue registering LOW (see Tb0).
3. After R_{TT} is switched off, disable write leveling mode via the MRS command (see Tc2).
4. After ^{t}MOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after ^{t}MRD [Td1]).

Figure 25: Write Leveling Exit

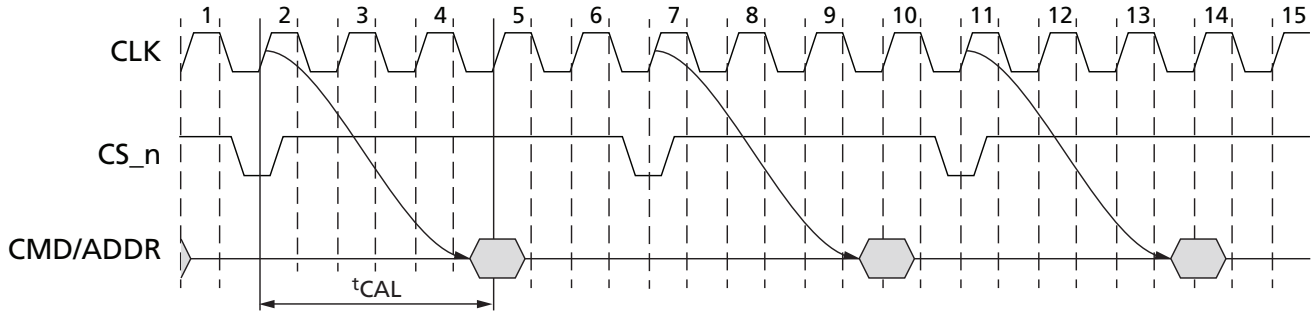


Notes: 1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS signals capturing CK_t HIGH just after the T0 state.
2. See previous figure for specific ^{t}WLO timing.

Command Address Latency

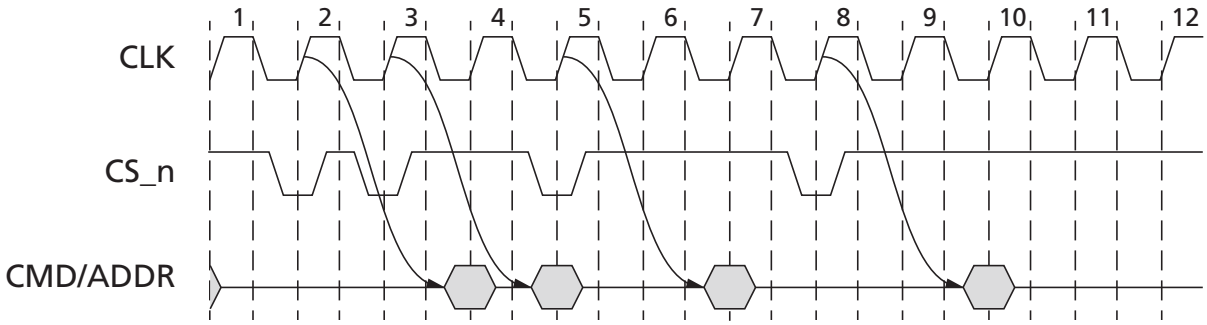
DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL timing is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL in clocks must be programmed into the mode register (see MR1 Register Definition table) and is based on the ^{t}CAL(ns)/^{t}CK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Figure 26: CAL Timing Definition



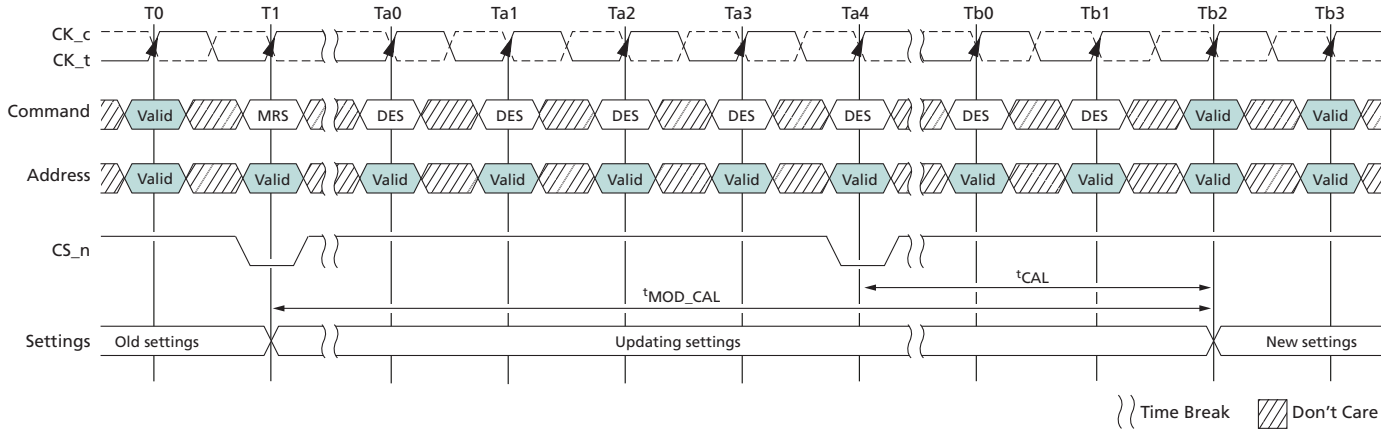
CAL gives the DRAM time to enable the command and address receivers before a command is issued. After the command and the address are latched, the receivers can be disabled if CS_n returns to HIGH. For consecutive commands, the DRAM will keep the command and address input receivers enabled for the duration of the command sequence.

Figure 27: CAL Timing Example (Consecutive CS_n = LOW)



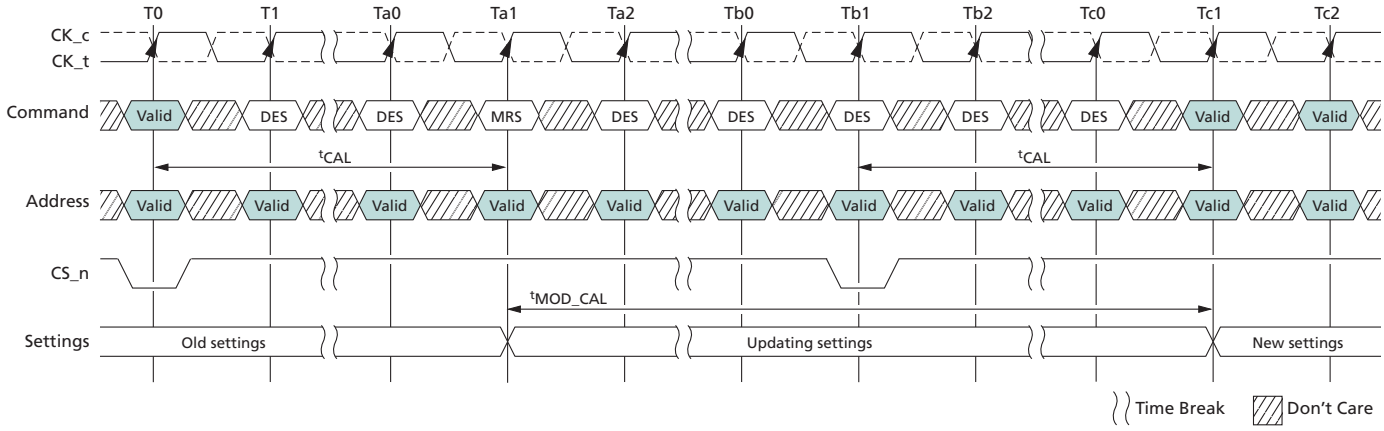
When the CAL mode is enabled, additional time is required for the MRS command to complete. The earliest the next valid command can be issued is ^{t}MOD_CAL, which should be equal to ^{t}MOD + ^{t}CAL. The two following figures are examples.

Figure 28: CAL Enable Timing – ^{t}MOD_CAL



Note: 1. CAL mode is enabled at T1.

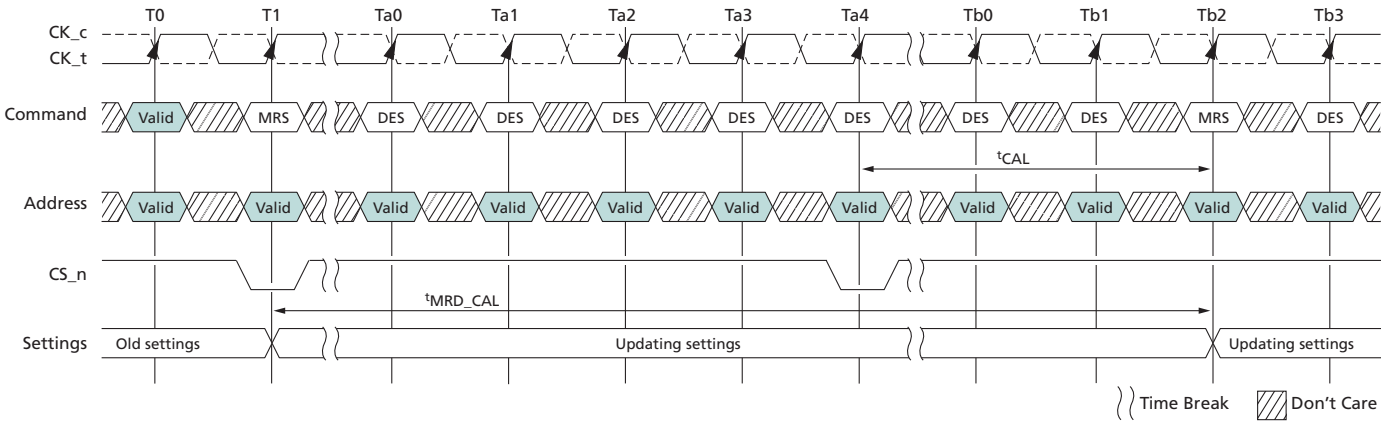
Figure 29: ^{t}MOD_CAL, MRS to Valid Command Timing with CAL Enabled



Note: 1. MRS at Ta1 may or may not modify CAL, ^{t}MOD_CAL is computed based on new ^{t}CAL setting if modified.

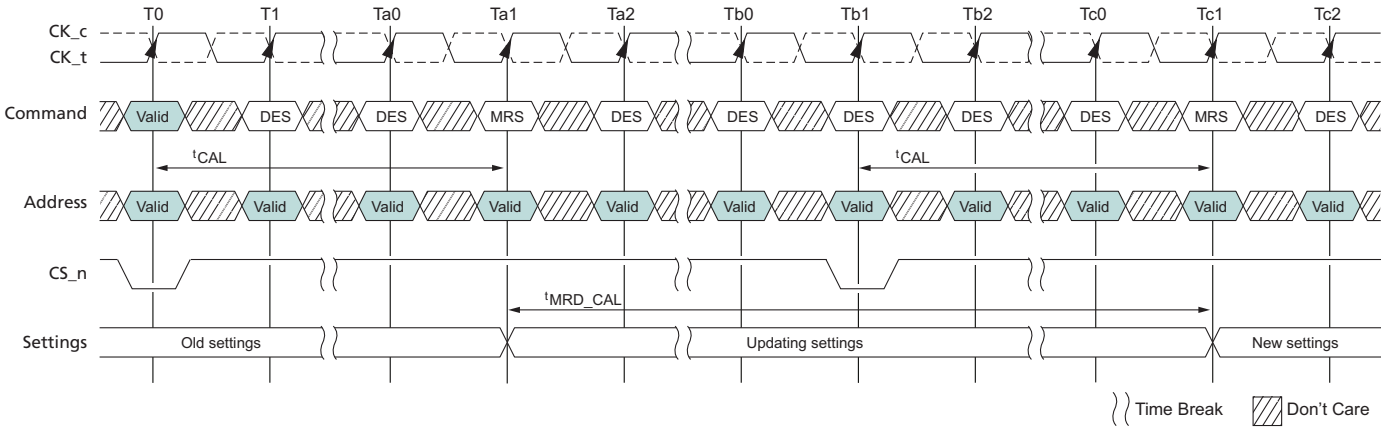
When the CAL mode is enabled or being enabled, the earliest the next MRS command can be issued is ^{t}MRD_CAL is equal to ^{t}MOD + ^{t}CAL. The two following figures are examples.

Figure 30: CAL Enabling MRS to Next MRS Command, ^{t}MRD_CAL



Note: 1. Command address latency mode is enabled at T1.

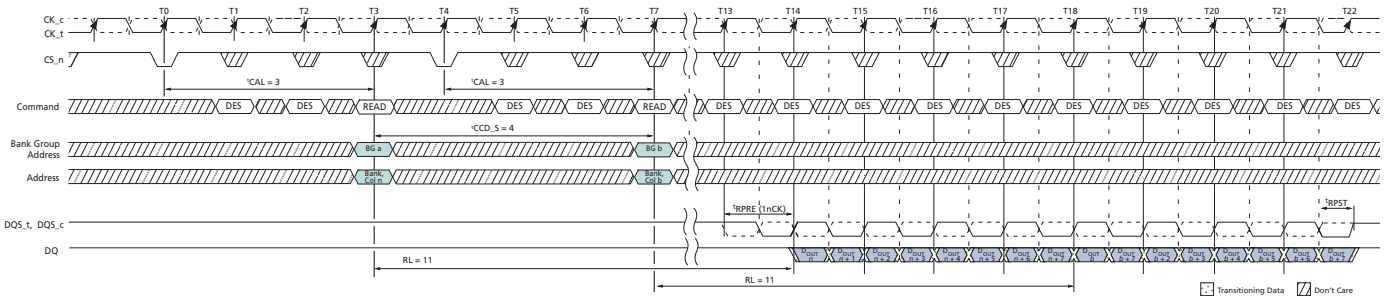
Figure 31: ^{t}MRD_CAL, Mode Register Cycle Time With CAL Enabled



Note: 1. MRS at Ta1 may or may not modify CAL, ^{t}MRD_CAL is computed based on new ^{t}CAL setting if modified.

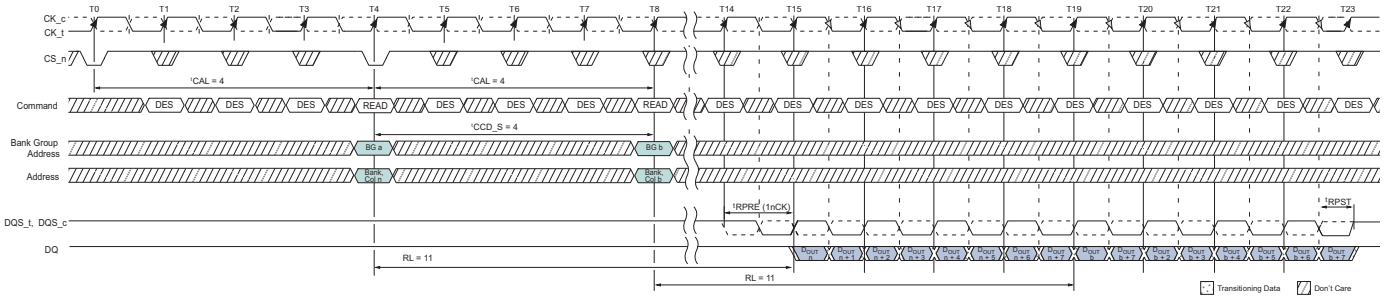
CAL Examples: Consecutive READ BL8 with two different CALs and 1^{t}CK preamble in different bank group shown in the following figures.

Figure 32: Consecutive READ BL8, CAL3, 1tCK Preamble, Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK.
2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T3 and T7.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

Figure 33: Consecutive READ BL8, CAL4, 1tCK Preamble, Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1tCK.
2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T4 and T8.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

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Low-Power Auto Self Refresh Mode

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

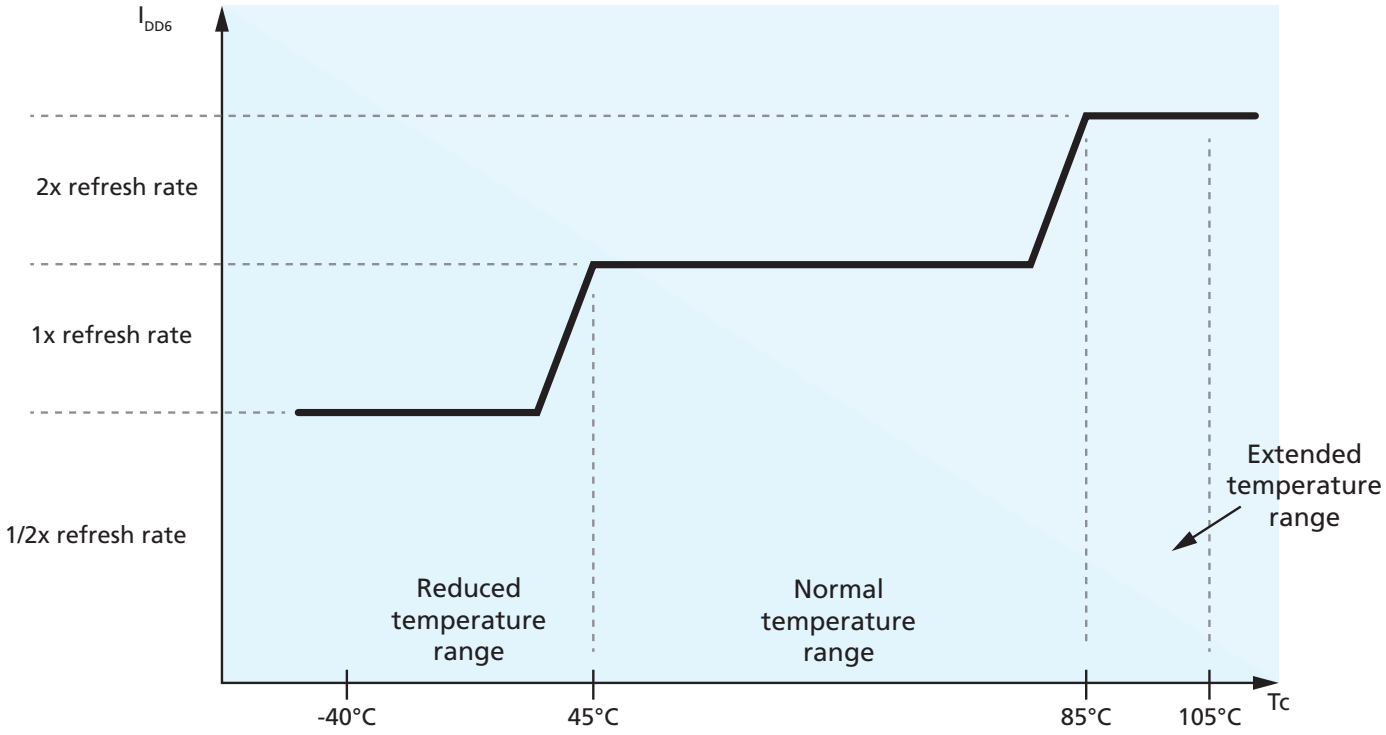
Manual Self Refresh Mode

If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible for maintaining the required memory temperature condition for the mode selected during the SELF REFRESH operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

Table 27: Auto Self Refresh Mode

MR2[7]	MR2[6]	Low-Power Auto Self Refresh Mode	SELF REFRESH Operation	Operating Temperature Range for Self Refresh Mode (DRAM T_{CASE})
0	0	Normal	Variable or fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	-40°C to 85°C
1	0	Extended temperature	Variable or fixed high self refresh rate optimizes data retention to support the extended temperature range.	-40°C to 105°C
0	1	Reduced temperature	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	-40°C to 45°C
1	1	Auto self refresh	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.	All of the above

Figure 34: Auto Self Refresh Ranges



Multipurpose Register

The MULTIPURPOSE REGISTER (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3. Page 0 can be read by any of three readout modes (serial, parallel, or staggered) while Pages 1, 2, and 3 can be read by only the serial readout mode. Page 3 is for DRAM vendor use only. MPR mode enable and page selection is done with MRS commands. Data bus inversion (DBI) is not allowed during MPR READ operation.

Once the MPR access mode is enabled (MR3[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and RESET; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. Power-down mode and SELF REFRESH command are not allowed during MPR enable mode. No other command can be issued within ^{t}RFC after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a REFRESH command.

Figure 35: MPR Block Diagram

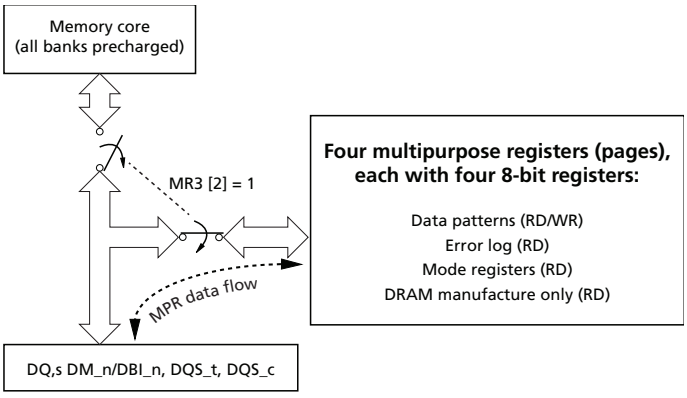


Table 28: MR3 Setting for the MPR Access Mode

Address	Operation Mode	Description
A[12:11]	MPR data read format	00 = Serial ..... 01 = Parallel 10 = Staggered .... 11 = Reserved
A2	MPR access	0 = Standard operation (MPR not enabled) 1 = MPR data flow enabled
A[1:0]	MPR page selection	00 = Page 0 .... 01 = Page 1 10 = Page 2 .... 11 = Page 3

Table 29: DRAM Address to MPR UI Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – A*x*	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UI*x*	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

Table 30: MPR Page and MPR*x* Definitions

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
MPR Page 0 – Read or Write (Data Patterns)										
BA[1:0]	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value listed)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	
MPR Page 1 – Read-only (Error Log)										
BA[1:0]	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-only
	01 = MPR1	CAS_n/A15	WE_n/A14	A13	A12	A11	A10	A9	A8	
	10 = MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/A16	
	11 = MPR3	CRC error status	CA parity error status CA parity latency: [5] = MR5[2], [4] = MR5[1], [3] = MR5[0]				C2	C1	C0	
MPR Page 2 – Read-only (MRS Readout)										
BA[1:0]	00 = MPR0	hPPR support	sPPR support	$R_{TT(WR)}$ MR2[11]	Temperature sensor status[2]		CRC write enable MR2[12]	$R_{TT(WR)}$ MR2[10:9]		Read-only
	01 = MPR1	V_{REFDQ} trainging range MR6[6]V_{REFDQ} training value: [6:1] = MR6[5:0]							Gear-down enable MR3[3]	
	10 = MPR2CAS latency: [7:3] = MR0[6:4,2,12]					CAS write latency [2:0] = MR2[5:3]				
	11 = MPR3$R_{TT(NOM)}$: [7:5] = MR1[10:8]			$R_{TT(Park)}$: [4:2] = MR5[8:6]			R_{ON}: [1:0] = MR1[2:1]			
MPR Page 3 – Read-only (Restricted, except for MPR3 [3:0])										
BA[1:0]	00 = MPR0	DC	DC	DC	DC	DC	DC	DC	DC	Read-only
	01 = MPR1	DC	DC	DC	DC	DC	DC	DC	DC	
	10 = MPR2	DC	DC	DC	DC	DC	DC	DC	DC	
	11 = MPR3	MBIST-PPR Support	DCMBIST-PPR Transparency			MAC	MAC	MAC	MAC	

Notes: 1. DC = "Don't Care"
2. MPR[4:3] 00 = Sub 1X refresh; MPR[4:3] 01 = 1X refresh; MPR[4:3] 10 = 2X refresh; MPR[4:3] 11 = Reserved

MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR READ operation; the device will ignore the Read DBI enable setting in MR5 [12] when in MPR mode. READ commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in . MPR page 0 can be rewritten via an MPR WRITE command. The

device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use ^{t}CCD_S or ^{t}CCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use ^{t}CCD_S timing between READ commands; ^{t}CCD_L must be used for timing between READ commands

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page *x*, MPR*y*).

1. The DLL must be locked if enabled.
2. Precharge all; wait until ^{t}RP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR read format, and MR3[1:0] MPR page.
   a) MR3[12:11] MPR read format:
      i) 00 = Serial read format
      ii) 01 = Parallel read format
      iii) 10 = staggered read format
      iv) 11 = RFU
   b) MR3[1:0] MPR page:
      i) 00 = MPR Page 0
      ii) 01 = MPR Page 1
      iii) 10 = MPR Page 2
      iv) 11 = MPR Page 3
4. ^{t}MRD and ^{t}MOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPR*x* location.
6. Issue RD or RDA command.
   a) BA1 and BA0 indicate MPR*x* location:
      i) 00 = MPR0
      ii) 01 = MPR1
      iii) 10 = MPR2
      iv) 11 = MPR3
   b) A12/BC = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
      i) If BL = 8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR READ commands.
   c) A2 = burst-type dependant:
      i) BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      ii) BL8: A2 = 1 not allowed
      iii) BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      iv) BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
   d) A[1:0] = 00, data burst is fixed nibble start at 00.
   e) Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."
7. After RL = AL + CL, DRAM bursts data from MPR*x* location; MPR readout format determined by MR3[A12,11,1,0].
8. Steps 5 through 7 may be repeated to read additional MPR*x* locations.

9. After the last MPR*x* READ burst, ^{t}MPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. After the ^{t}MOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR Readout Format

The MPR read data format can be set to three different settings: serial, parallel, and staggered.

MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MR*x*, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).

Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

Table 31: MPR Readout Serial Format

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
x4 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
x8 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
x16 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

Table 31: MPR Readout Serial Format (Continued)

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Table 32: MPR Readout – Parallel Format

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
x4 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
x8 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
x16 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1

Table 32: MPR Readout – Parallel Format

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations. For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on, as shown below. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on. Examples of different starting locations are also shown.

Table 33: MPR Readout Staggered Format, x4

x4 READ MPR0 Command		x4 READ MPR1 Command		x4 READ MPR2 Command		x4 READ MPR3 Command	
Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]	Stagger	UI[7:0]
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

Table 34: MPR Readout Staggered Format, x4 – Consecutive READs

Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

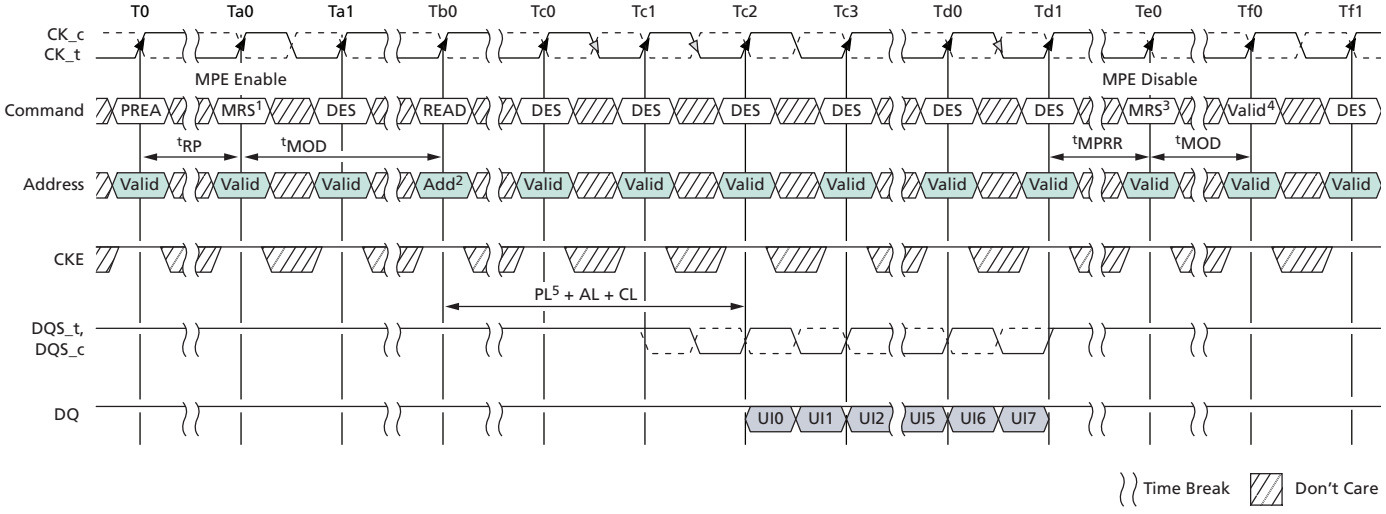
Table 35: MPR Readout Staggered Format, x8 and x16

x8 READ MPR0 Command		x16 READ MPR0 Command		x16 READ MPR0 Command	
Stagger	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

MPR READ Waveforms

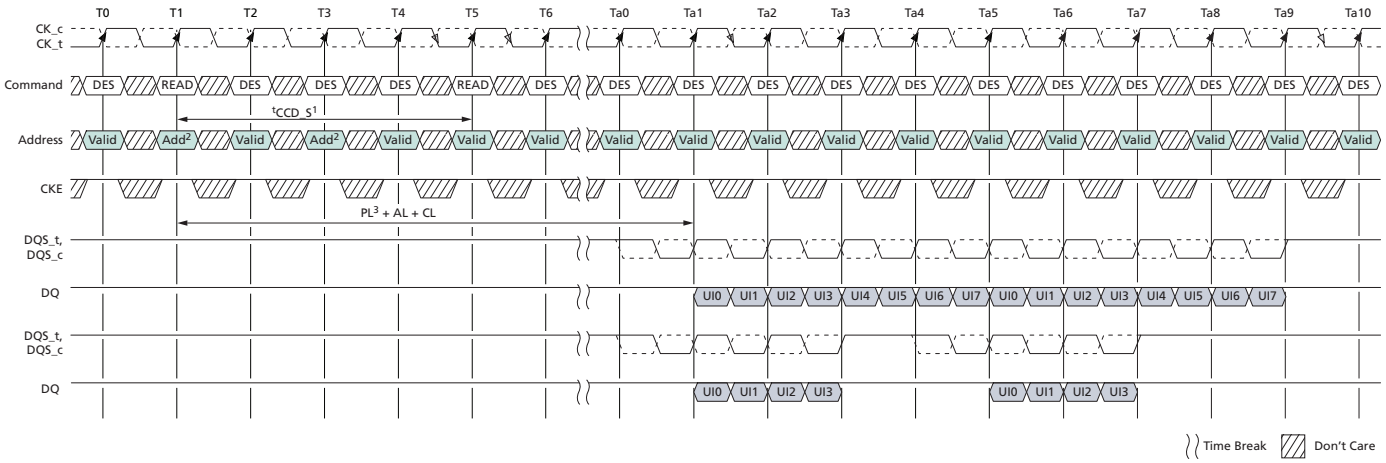
The following waveforms show MPR read accesses.

Figure 36: MPR READ Timing



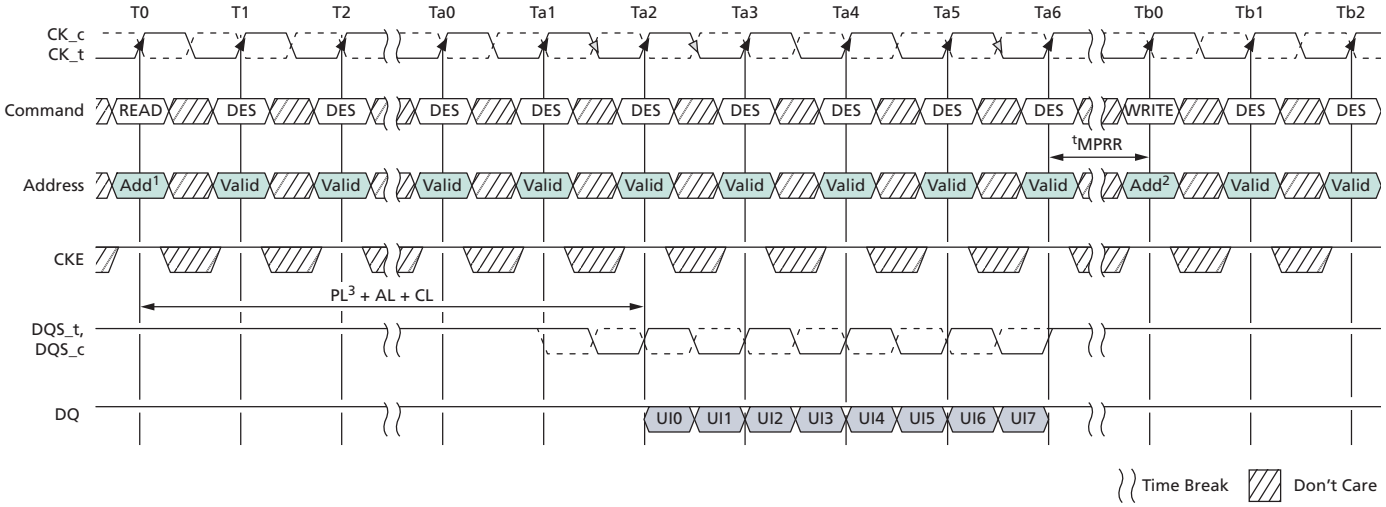
Notes: 1. ^{t}CCD_S = 4^{t}CK, Read Preamble = 1^{t}CK.
2. Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Multipurpose registers read/write disable (MR3 A2 = 0).
4. Continue with regular DRAM command.
5. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 37: MPR Back-to-Back READ Timing



Notes: 1. $^{t}CCD\_S = 4^{t}CK$, Read Preamble = $1^{t}CK$.
2. Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T, T)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 38: MPR READ-to-WRITE Timing



Notes: 1. Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 and must be 1b when MR0 A[1:0] = 01
2. Address setting:
BA1 and BA0 indicate the MPR location
A[7:0] = data for MPR
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care"

3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

MPR Writes

MPR access mode allows 8-bit writes to the MPR Page 0 using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR WRITE operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

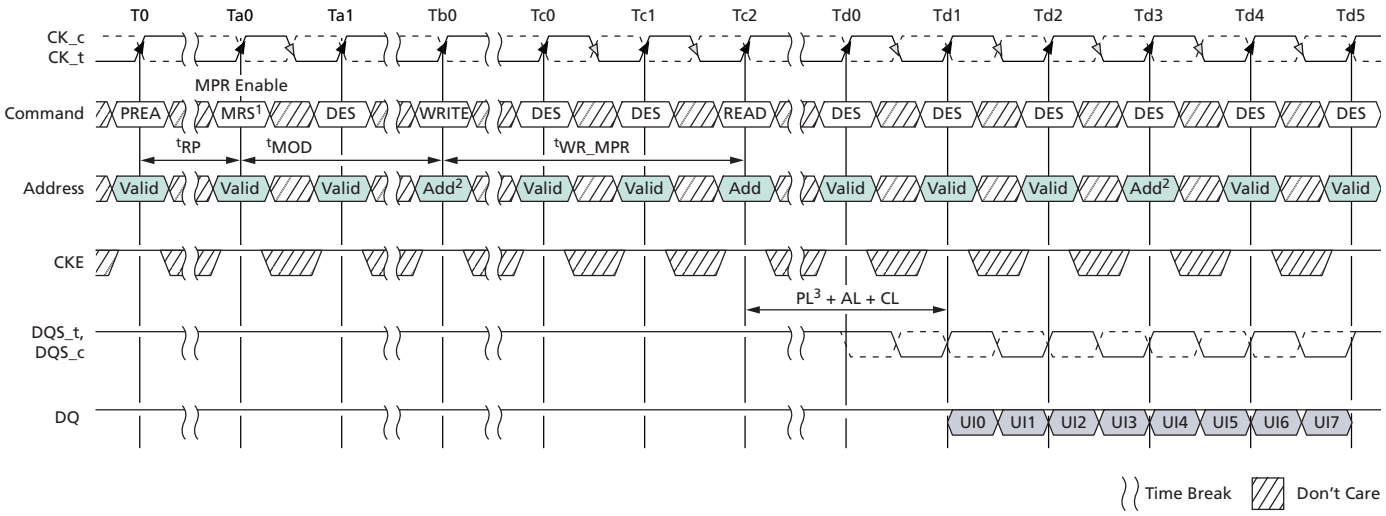
The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked if enabled.
2. Precharge all; wait until ^{t}RP is satisfied.
3. MRS command to MR3[2] = 1 (enable MPR data flow) and MR3[1:0] = 00 (MPR Page 0); writes to 01, 10, and 11 are not allowed.
4. ^{t}MRD and ^{t}MOD must be satisfied.
5. Redirect all subsequent WRITE commands to specific MPR*x* location.
6. Issue WR or WRA command:
   a) BA1 and BA0 indicate MPR*x* location
      i) 00 = MPR0
      ii) 01 = MPR1
      iii) 10 = MPR2
      iv) 11 = MPR3
   b) A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
   c) Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."
7. ^{t}WR_MPR must be satisfied to complete MPR WRITE.
8. Steps 5 through 7 may be repeated to write additional MPR*x* locations.
9. After the last MPR*x* WRITE, ^{t}MPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. When the ^{t}MOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR WRITE Waveforms

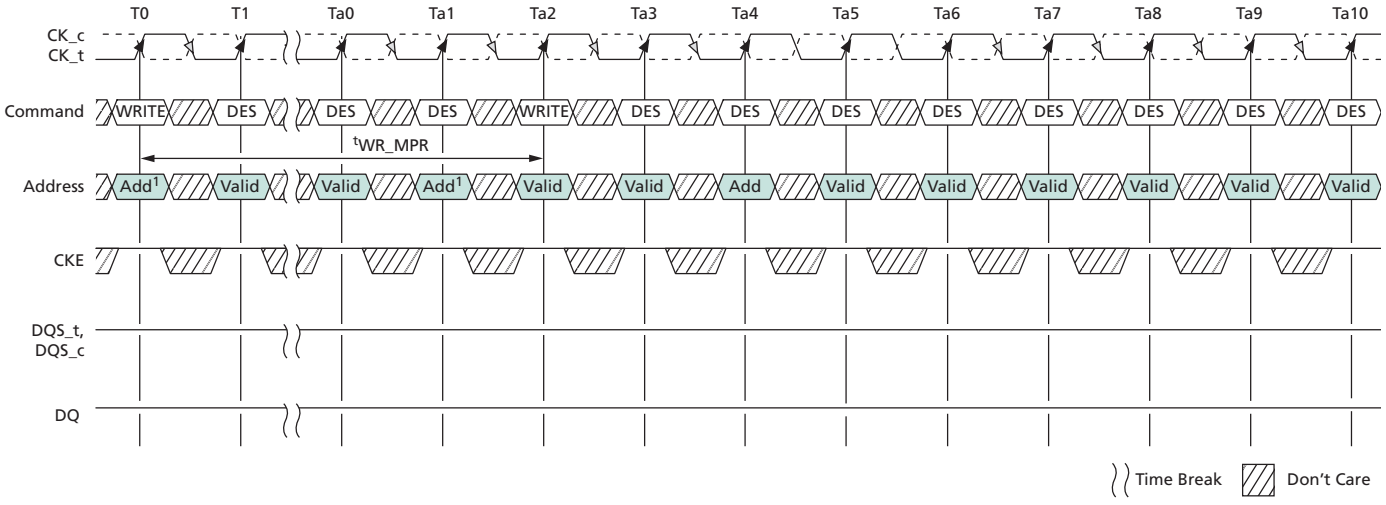
The following waveforms show MPR write accesses.

Figure 39: MPR WRITE and WRITE-to-READ Timing



Notes: 1. Multipurpose registers read/write enable (MR3 A2 = 1).
2. Address setting:
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care"
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 40: MPR Back-to-Back WRITE Timing

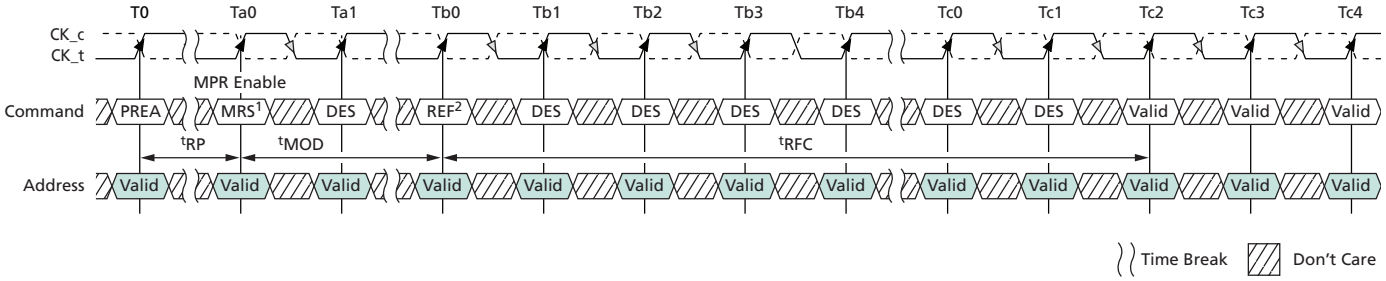


Note: 1. Address setting:
BA1 and BA0 indicate the MPR location
A[7:0] = data for MPR
A10 and other address pins are "Don't Care"

MPR REFRESH Waveforms

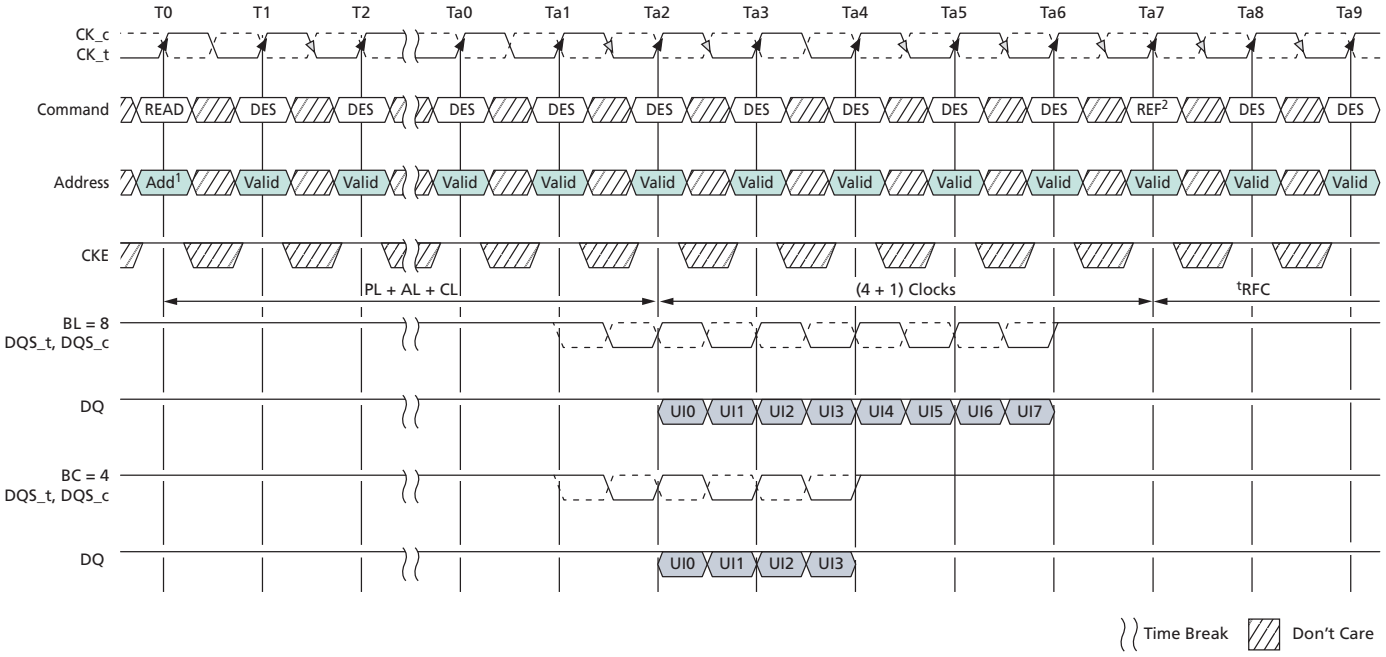
The following waveforms show MPR accesses interaction with refreshes.

Figure 41: REFRESH Timing



Notes: 1. Multipurpose registers read/write enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.
2. 1x refresh is only allowed when MPR mode is enabled.

Figure 42: READ-to-REFRESH Timing



Notes: 1. Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
2. 1x refresh is only allowed when MPR mode is enabled.