

Inductorless, Dual Output **Off-Line Regulators**

Features

- Accepts peak input voltages up to 700V
- Operates directly off of rectified 120 or 230VAC
- Integrated linear regulator
- Minimal power dissipation
- No high voltage capacitors required
- No transformers or inductors required
- Up to 1.0W output power

Applications

- 3.3V power supplies
- SMPS house keeping power supplies
- White goods
- Appliances
- Small off-line low voltage power supplies
- Lighting controls

Typical Application Circuit

General Description



The Supertex SR036 is an inductorless, dual output off-line controller providing up to 1.0W of output power. It does not require any transformers, inductors, or high voltage input capacitors. The input voltage, HV_{IN}, is designed to operate from an unfiltered full wave rectified 120V or 230V AC line. It is designed to control an external N-channel MOSFET or IGBT. When HV_{IN} is less than 45V, the external transistor is turned-on, allowing it to charge an external capacitor connected to V_{SOURCE}. An unregulated DC voltage will develop on V_{SOURCE}. Once HV_{IN} is above 45V, the transistor is turned off. The maximum gate voltage for the external transistor is 24V. The unregulated voltage is approximately 18V. The SR036 also provides a regulated 3.3V.

WARNING! Galvanic isolation is not provided. Dangerous voltages are present when connected to the AC line. It is the responsibility of the designer to assure adequate safeguards are in place to protect the end user from





Electrical Specifications (Over operating supply voltages unless otherwise noted, $T_A = 0^{\circ}C$ to +125°C)

Sym	Parameter	Min	Тур	Max	Units	Conditions
HV _{IN}			-	700	V	Peak transient voltage
	Input voltage	-	-	407	V	Peak rectified AC voltage
V _{TH}	HV _{IN} voltage when Gate is pulled to ground	40	45	50	V	
V _{GS}	Gate to Source clamp voltage	±10	±15	±20	V	Ι _{GS} = ±100μΑ
V _{GATE}	Gate to ground clamp voltage	18	20	24	V	
V _{OUT}	Regulated output voltage for the 8-Lead SOIC	2.97	3.30	3.63	V	V _{SOURCE} = 10V
ΔV _{OUT}	V _{out} load regulation	-	20	120	mV	V_{SOURCE} = 10V, I_{LOAD} = 0 to 50mA ¹
Freq	Input AC frequency	40	-	100	Hz	

1. Load current on the regulated output must not cause power dissipation to exceed max ratings. Worst case power dissipation is given by:

$$\mathsf{P} \approx \frac{\mathsf{V}_{\mathsf{IN}}^{2}}{185 \mathrm{k}\Omega} + (16 \mathrm{V} - \mathrm{V}_{\mathsf{OUT}}) \bullet \mathsf{I}_{\mathsf{OUT}}$$

Where I_{out} is the load on the regulated output.

Typical Performance Curves



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Power dissipation

Application Information

Power dissipation in the SR036 is from 2 sources. The first is due to the bias current (or overhead) required to operate the device. This may be calculated from $P_{BIAS} = V_{IN}^{2}/185 k\Omega$, where V_{IN} is the input voltage in V_{RMS} . The second source of power dissipation is the 3.3V linear regulator and may be calculated from $P_{REG} = (16V - V_{OUT}) * I_{REG}$, where V_{OUT} is 3.3V, and I_{REG} is the load current on the 3.3V output. The total power dissipated by the SR036 is the sum of these two: $P_{BIAS} + P_{REG}$. (These equations are conservative – actual dissipation may be less.)

To adequately dissipate the power, the underside plate of the SR036SG should be soldered to at least 2.0cm² of exposed copper area on the PCB.

Functional Block Diagram

Power is also dissipated by the pass transistor. Power dissipated by the transistor will be $(16V * I_{TOTAL}) * (1/Eff - 1)$ where I_{TOTAL} is the sum of the load currents on the regulated and unregulated outputs and Eff is the converter efficiency (0.30 to be conservative). The transistor should be soldered to at least 5.0 cm² of exposed copper area on the PCB for heat-sinking.

Transformers



Do not use a transformer - either fixed or variable - on the AC line. The inductance of the transformer interferes with the normal operation of the SR036.

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SR036 Circuit Using VN2460 (with EMI Supression Circuit)

120VAC/60Hz - Limits per 47CFR15.107 for Class B devices. 45mA total load.



SR036 Circuit Using GN2470 (no EMI Supressor)

120VAC/60Hz - Limits per 47CFR15.107 for Class B devices. 50mA total load.



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SR036 Circuit Using GN2470 (no EMI Supressor)

120VAC/60Hz - Limits per 47CFR15.107 for Class B devices. 100mA total load.



Application Information (cont.)



Figure 2: Example Circuit with Enable Control

Figure 2 is an example circuit using the SR036 along with a Supertex GN2470 IGBT to generate an unregulated voltage of approximately 18V and a regulated voltage of 3.3V. The combined total output current is typically 50mA. The TN2106K1 in series with a $1.0K\Omega$ resistor can be added for applications requiring an enable control.



Figure 3: Generating Two Regulated Voltages

For applications requiring two regulated voltages, an inexpensive discrete linear regulator can be added to regulate the unregulated output as show in Figure 3. The discrete linear regulator consists of a Zener diode, a resistor and a bipolar transistor. The regulated voltage, V_{out} 1, is determined

by the Zener diode voltage minus the base-to-emitter voltage drop of 0.6V. Figure 3 uses a 5.6V Zener diode to obtain a 5.0V output. Different Zener diode voltages can be used to obtain different regulated output voltages.



The circuit shown in Figure 4 uses the SR036 to supply a regulated 3.3V for the logic control circuitry, while the unregulated voltage is used to drive a 12V relay coil. The operat-

ing voltage for a 12V relay coil is typically very wide and can therefore operate directly from the unregulated line.

Application Information (cont.)



2. The LED current is regulated at up to 40mA.

3. The LED string voltage can be up to AC line voltage (120V for 120VAC / 230V for 230VAC).

Application Information (cont.)



8-Lead MSOP Package Outline (MG) 3.00x3.00mm body, 1.10mm height (max), 0.65mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		Α	A1	A2	b	D	E	E1	е	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.22	2.80*	4.65*	2.80*		0.40	0.95 REF	0.25 BSC	0 0	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00	0.65 BSC	1 0 60 1			-	-
	MAX	1.10	0.15	0.95	0.38	3.20*	5.15*	3.20*	200				8 0	15 ⁰

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings are not to scale.

Supertex Doc. #: DSPD-8MSOPMG, Version G101008.

8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG) 4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



Notes:

1. If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/ identifier; an embedded metal marker; or a printed indicator.

Symbol		Α	A1	A2	b	D	D1	E	E1	E2	е	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30†	5.80*	3.80*	2.29†		0.25 -	0.40	1.04 REF	0.25 BSC	0 0	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-	1.27 BSC		-			-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81 [†]	6.20*	4.00*	2.79†	0.50	1.27		500	8 0	15 ⁰	

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.

* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc. #: DSPD-8SOSG, Version C090408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <u>http://www.supertex.com/packaging.html</u>.)

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