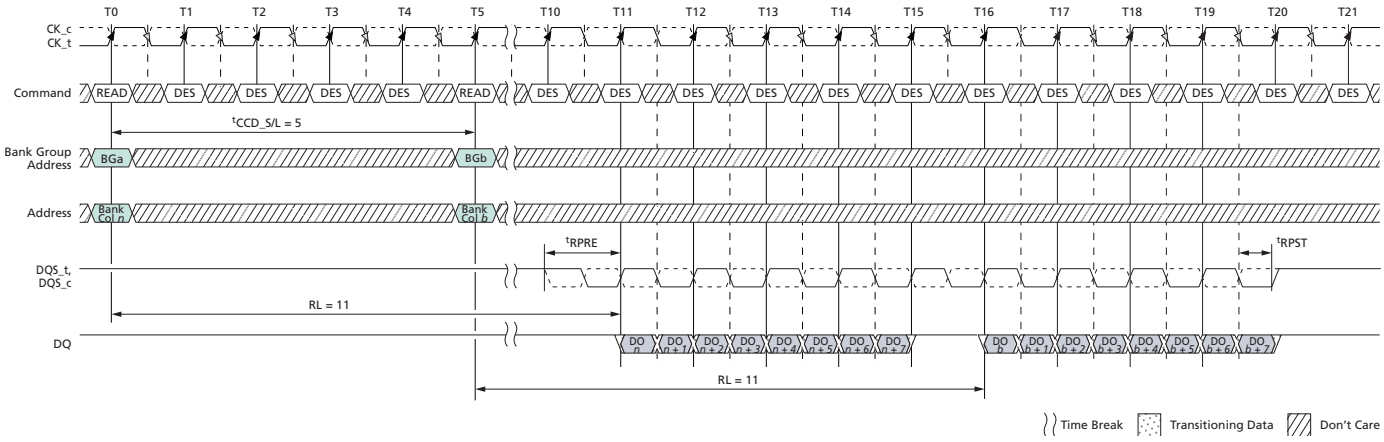
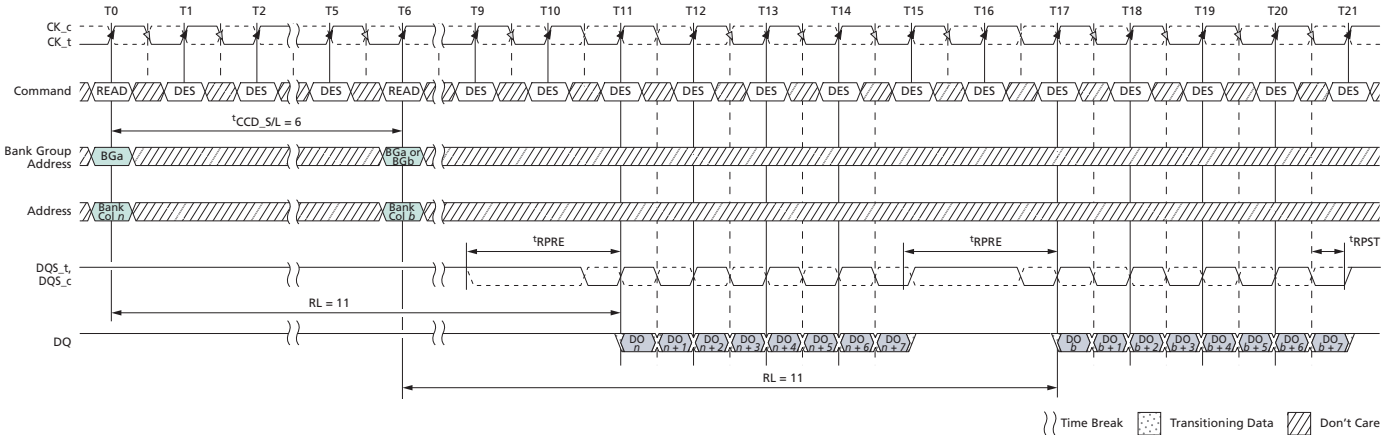
Figure 135: Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



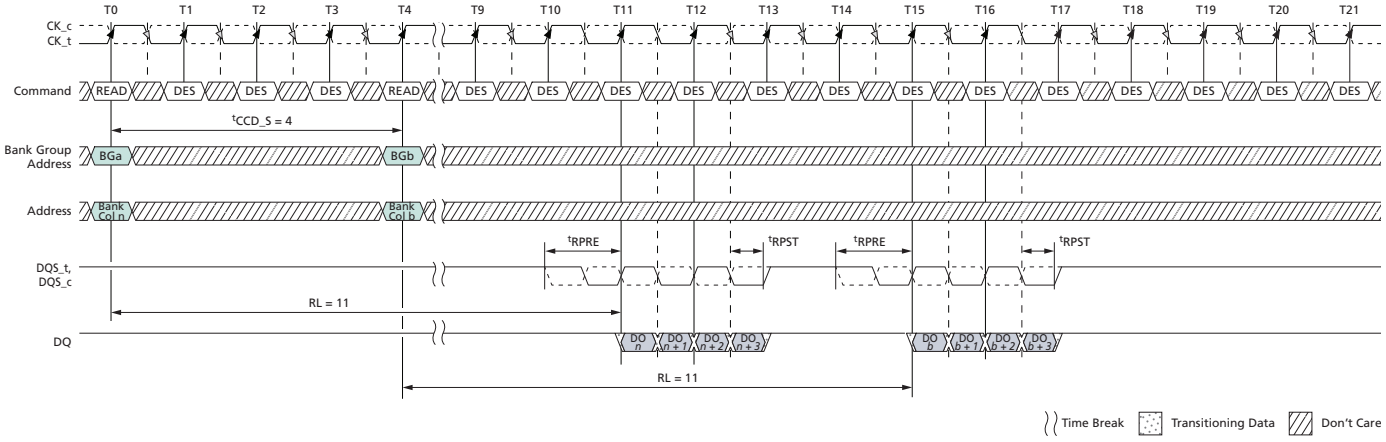
Notes: 1. BL8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 136: Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



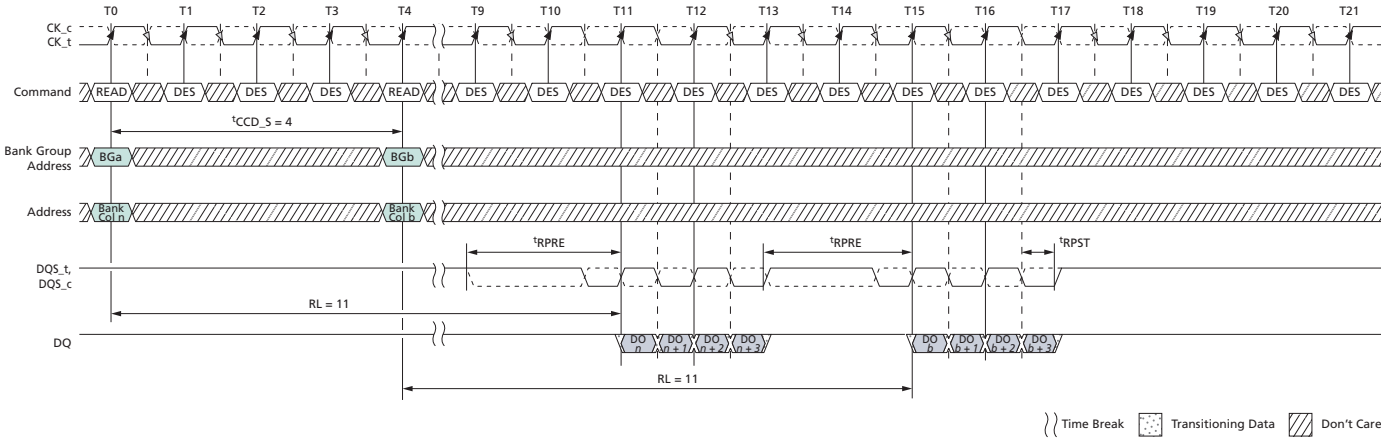
Notes: 1. BL8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.
6. 6 tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

Figure 137: READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



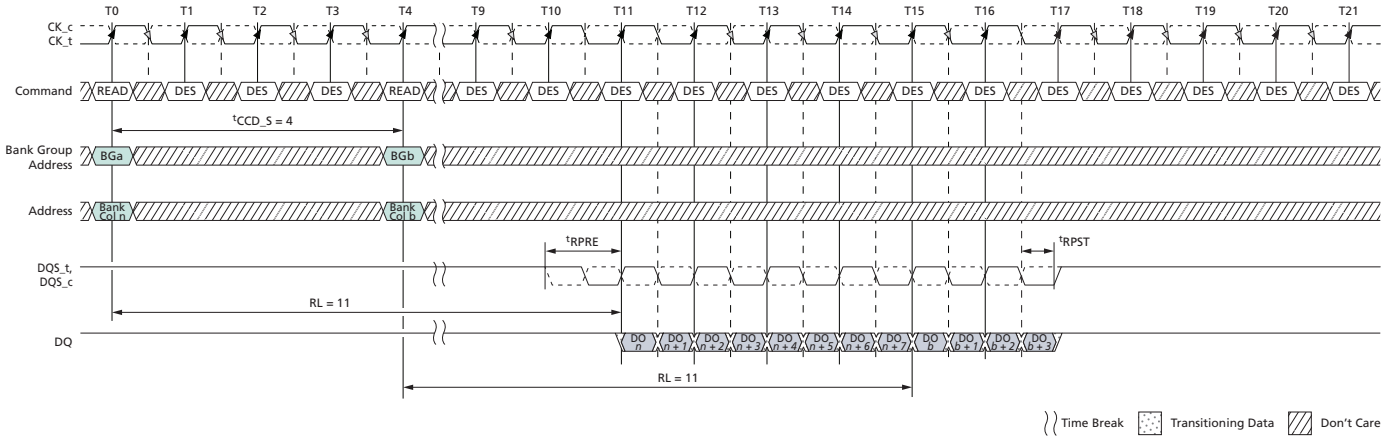
Notes: 1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 138: READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



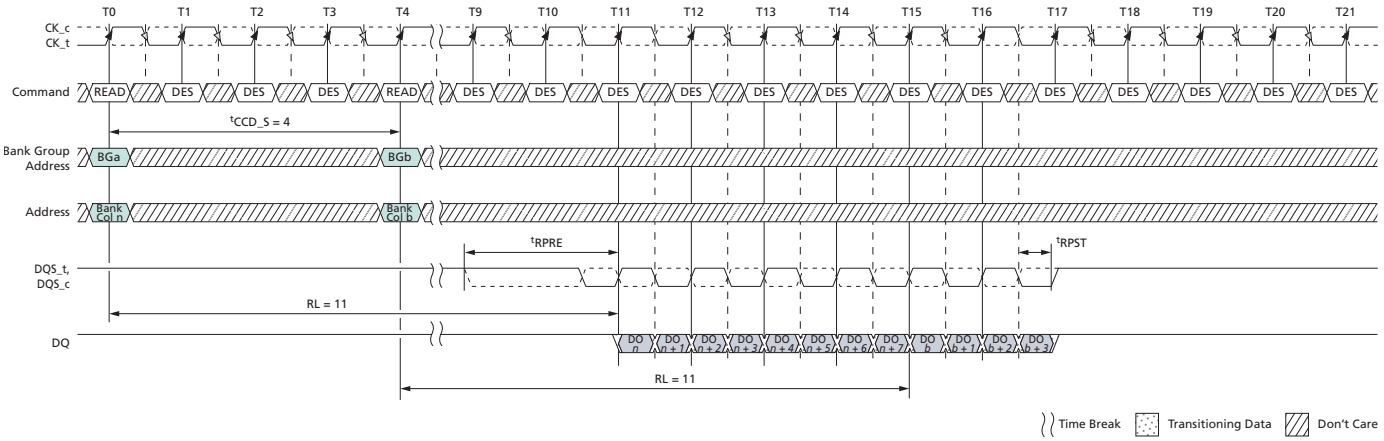
Notes: 1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 139: READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



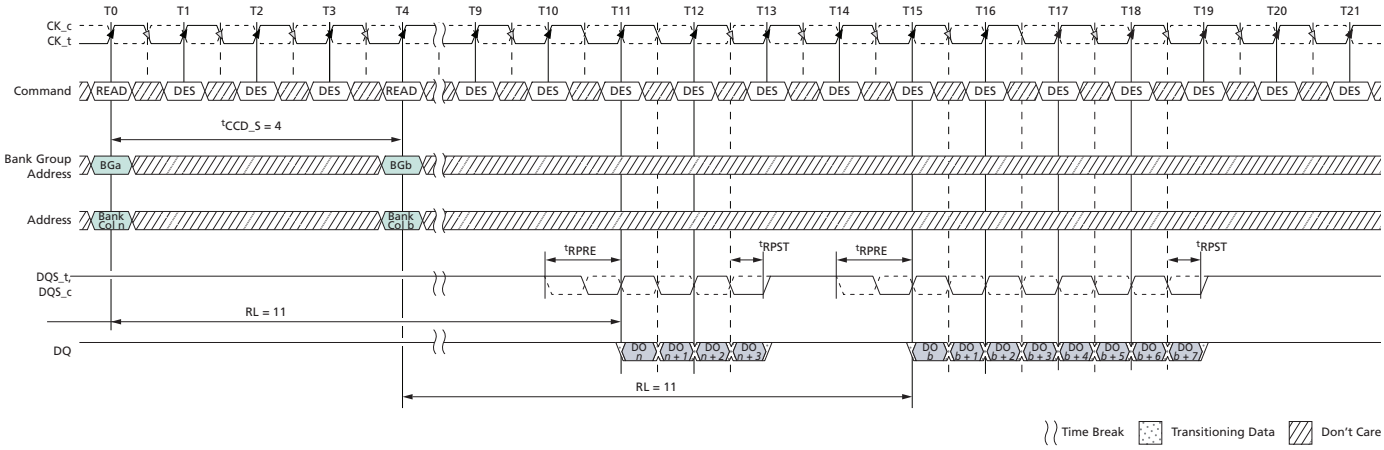
Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 140: READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



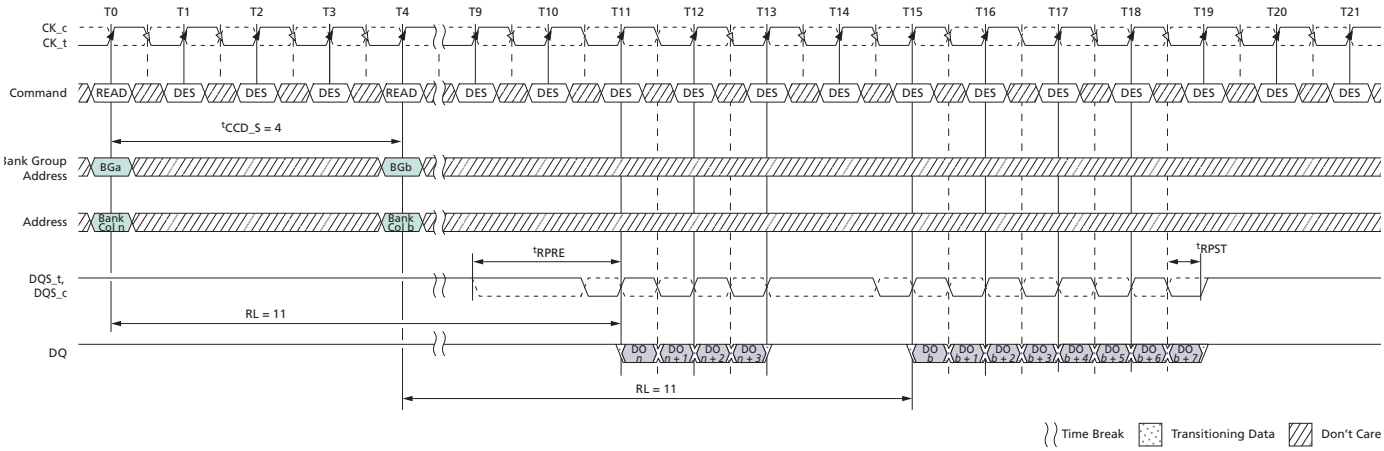
Notes: 1. BL = 8, AL =0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 141: READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



Notes: 1. BL = 8, AL =0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

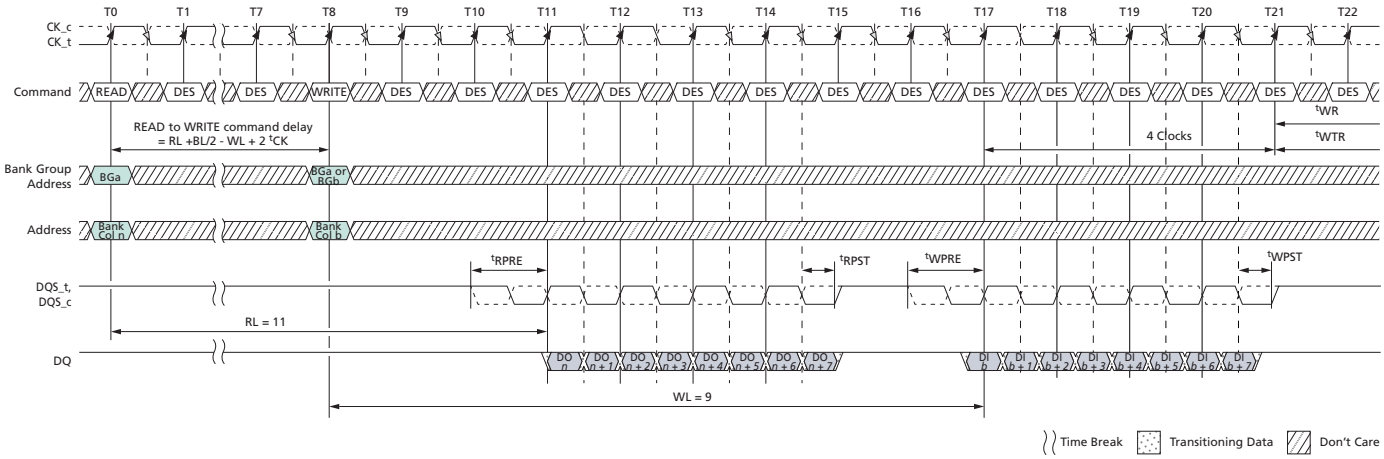
Figure 142: READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

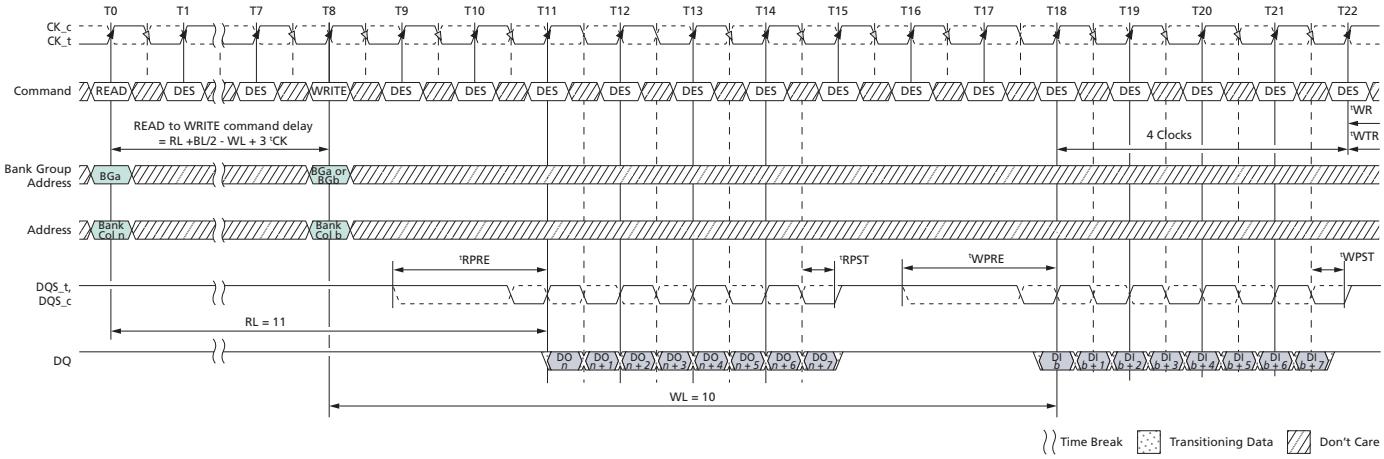
READ Operation Followed by WRITE Operation

Figure 143: READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



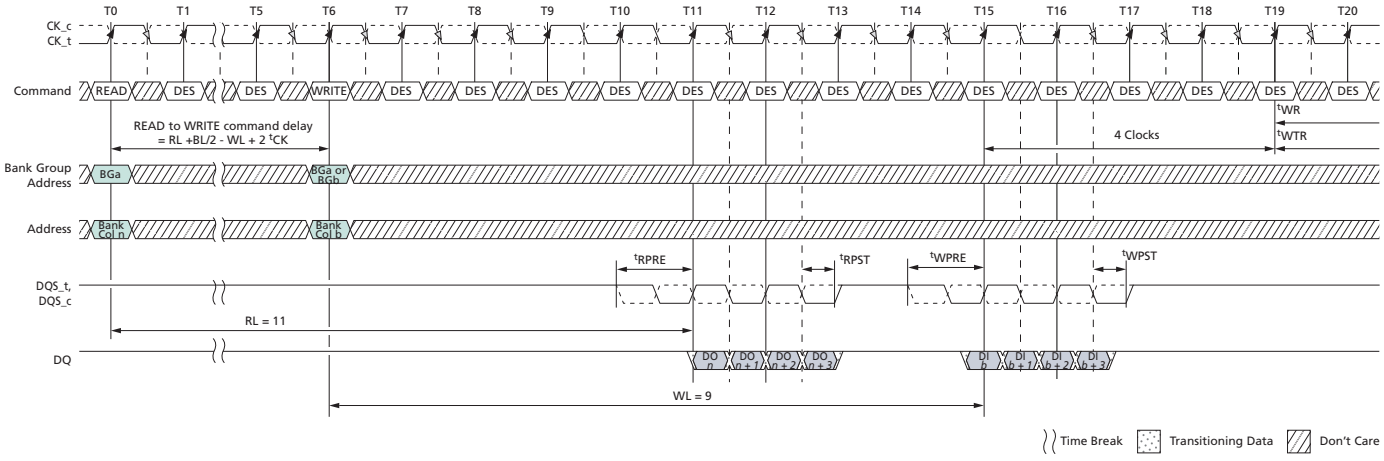
Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 144: READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



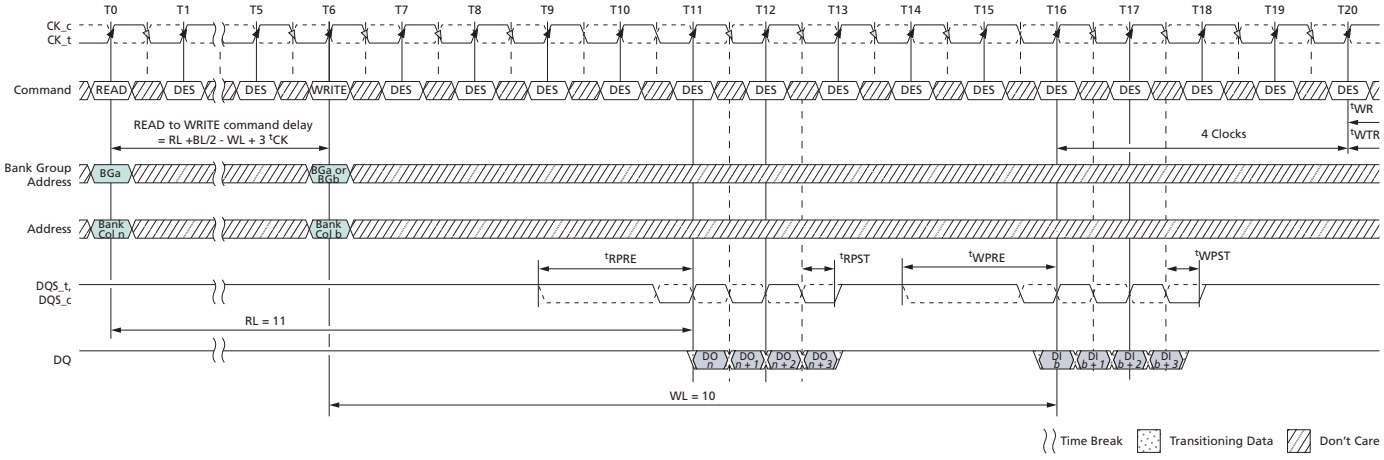
Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9+1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 145: READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



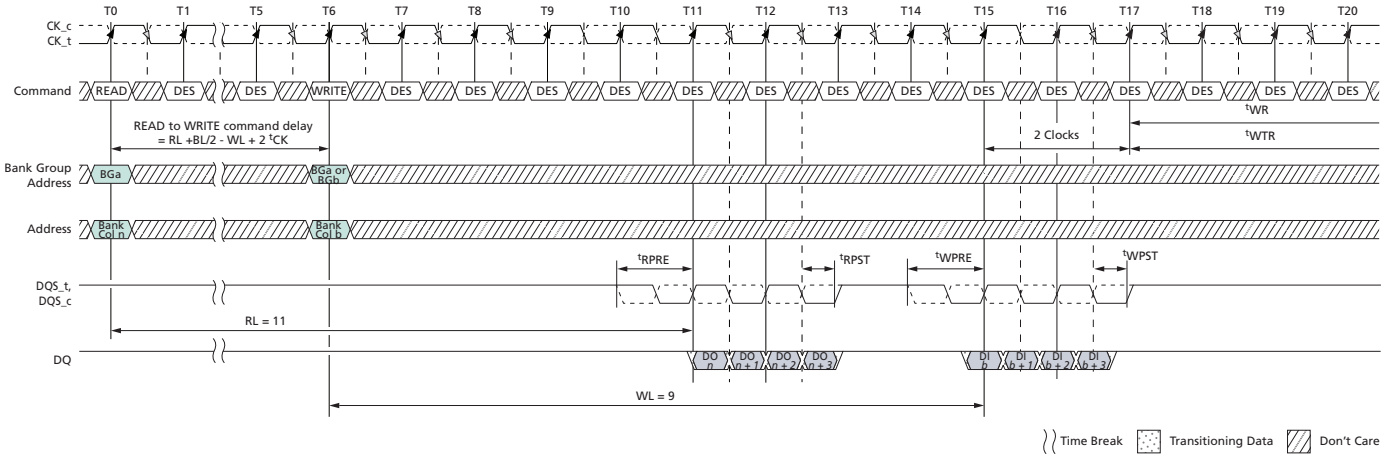
Notes: 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 146: READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



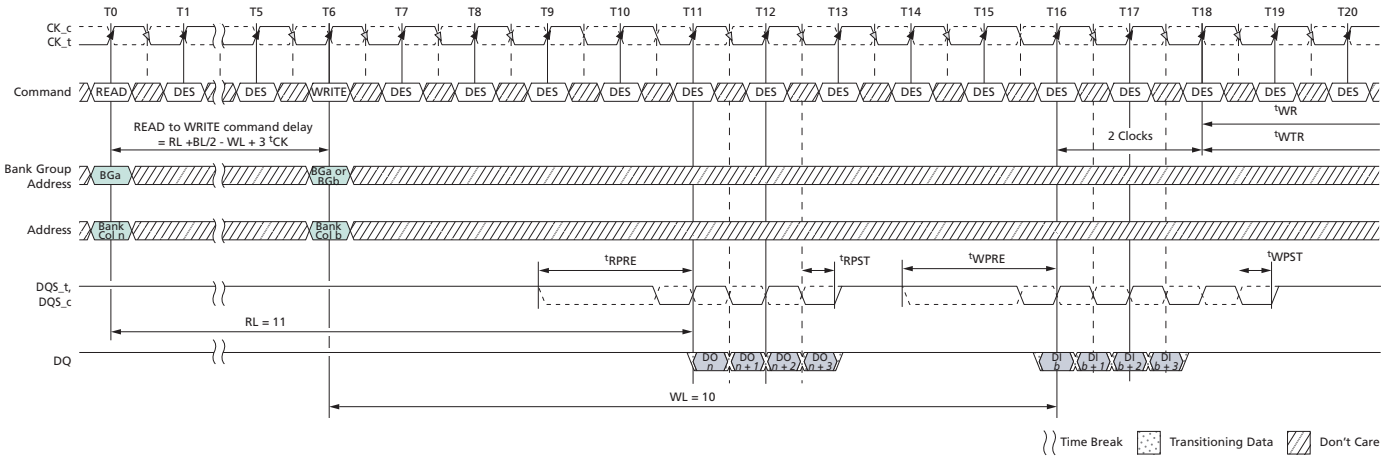
Notes: 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 147: READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



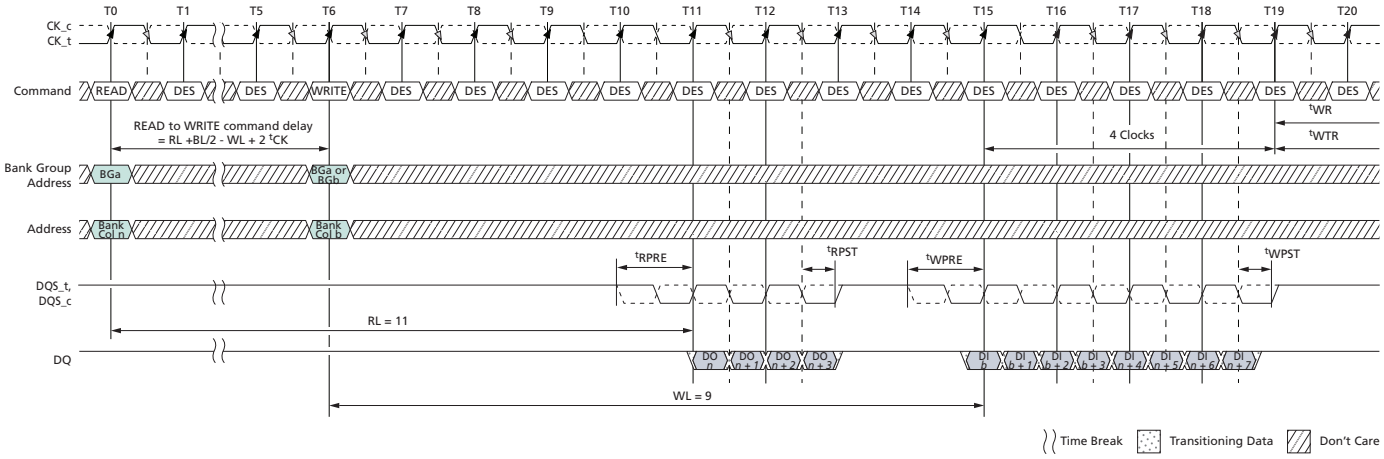
Notes: 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 01.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 148: READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



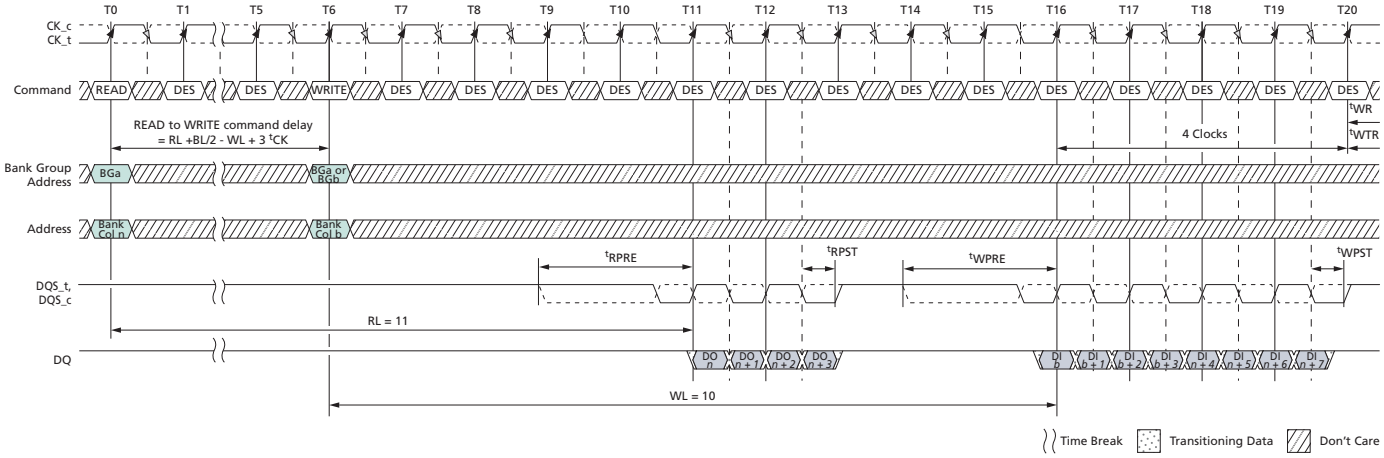
Notes: 1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 9 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 10.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 149: READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



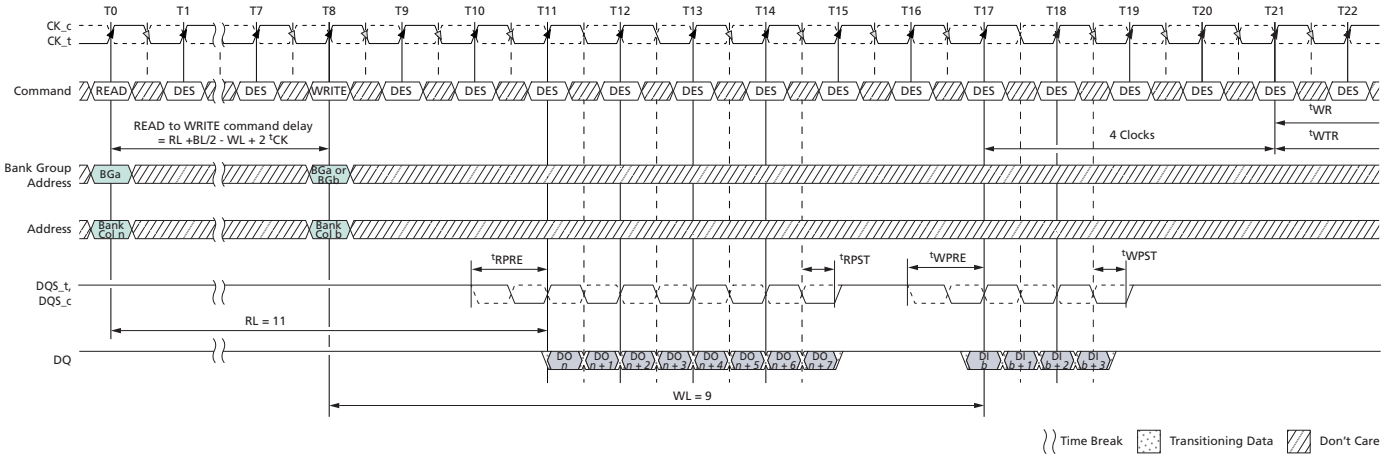
Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0.
BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 150: READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



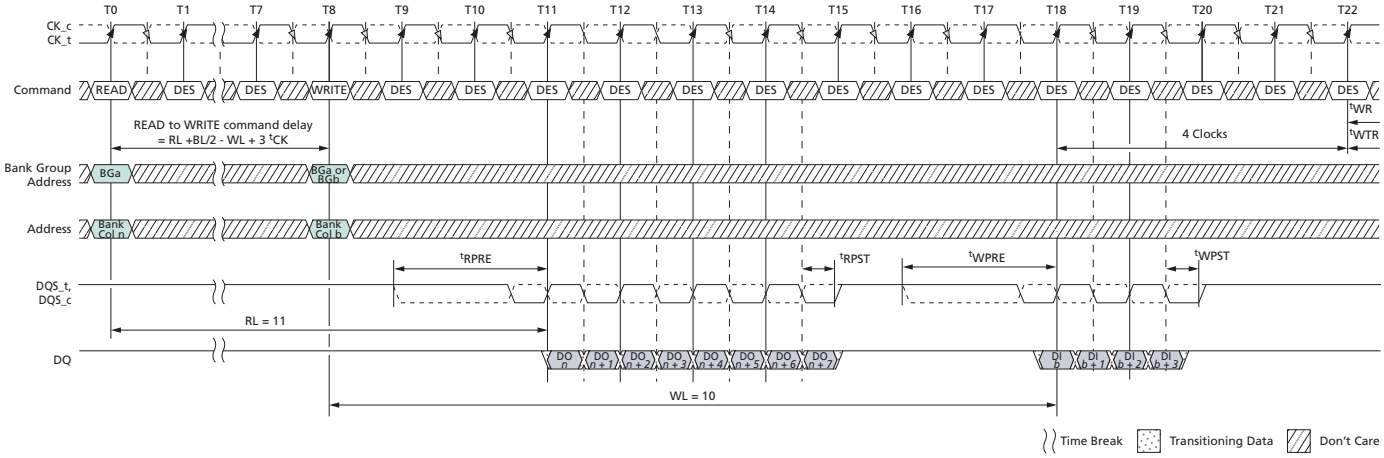
Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0.
BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 151: READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0.
BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 152: READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0.
BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

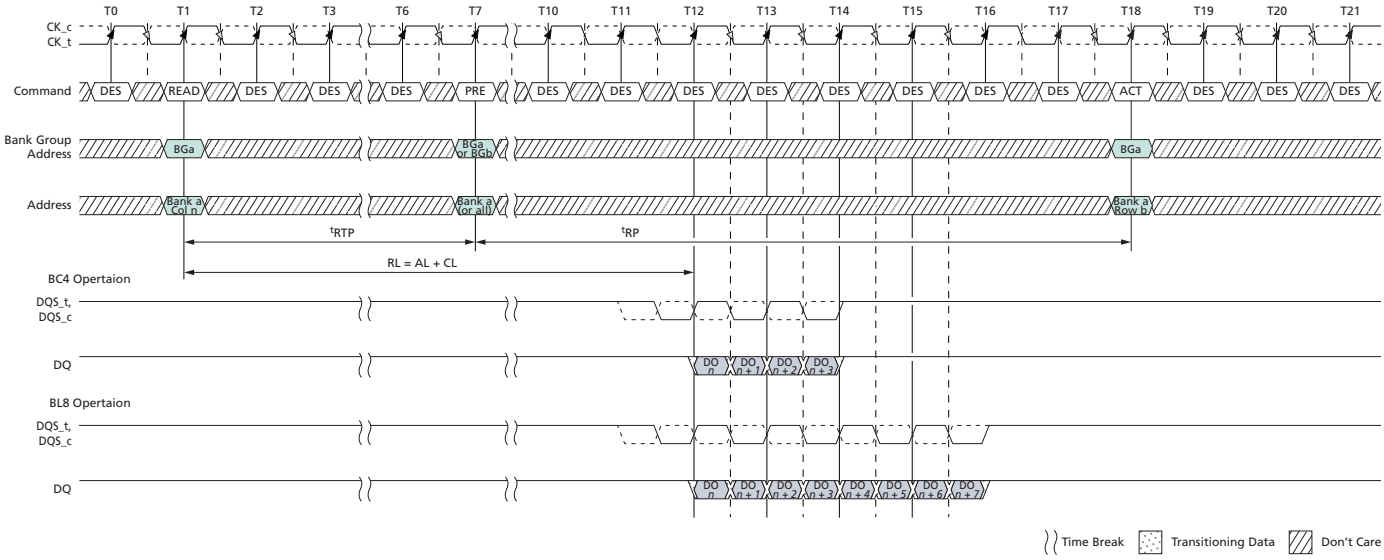
READ Operation Followed by PRECHARGE Operation

The minimum external READ command to PRECHARGE command spacing to the same bank is equal to AL + tRTP with tRTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the internal

READ command to PRECHARGE command delay is given by ^{t}RTP (MIN) = MAX (4 × *n*CK, 7.5ns). A new bank ACTIVATE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

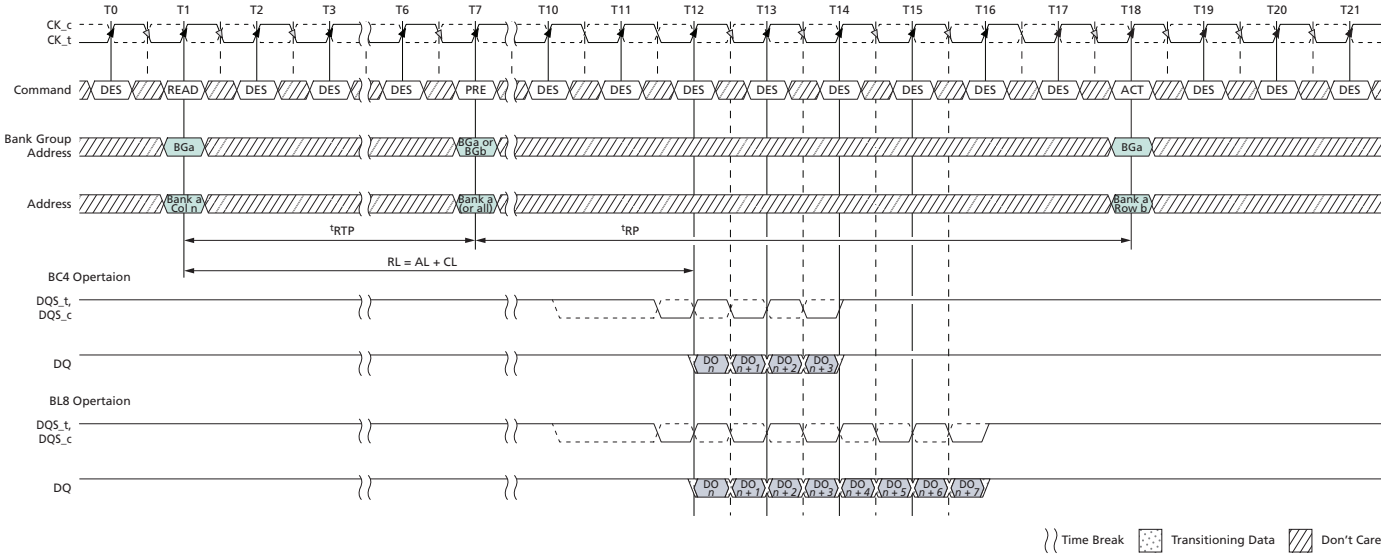
- The minimum RAS precharge time (^{t}RP [MIN]) has been satisfied from the clock at which the precharge begins.
- The minimum RAS cycle time (^{t}RC [MIN]) from the previous bank activation has been satisfied.

Figure 153: READ to PRECHARGE with 1^{t}CK Preamble



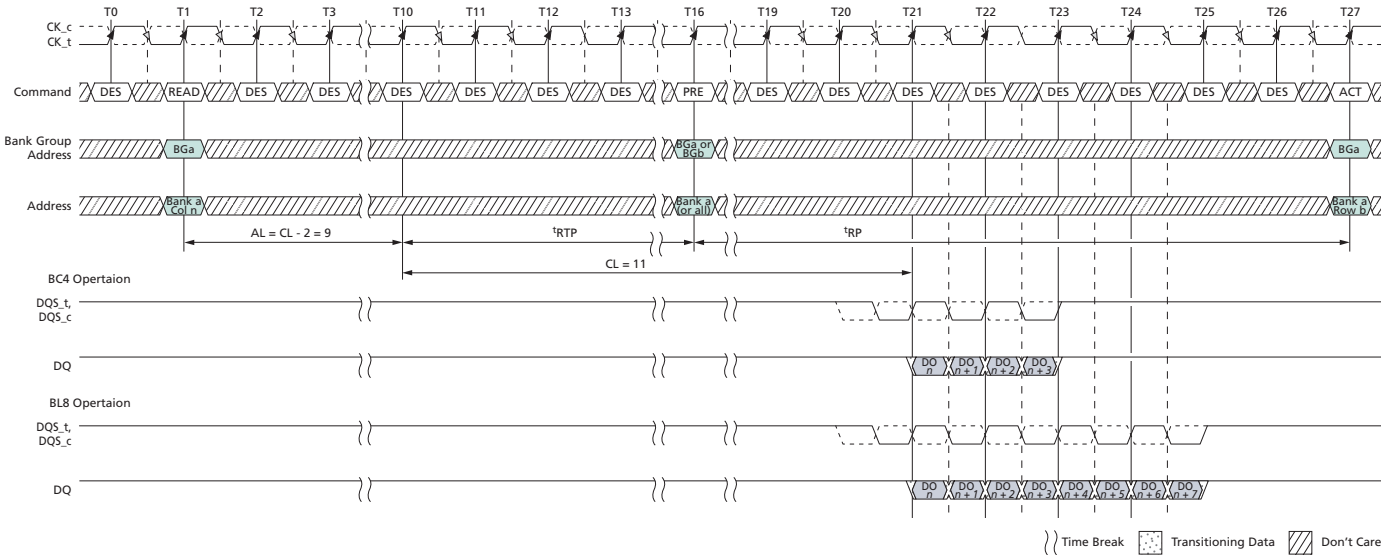
Notes: 1. RL = 11 (CL = 11, AL = 0), Preamble = 1^{t}CK, ^{t}RTP = 6, ^{t}RP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes that ^{t}RAS (MIN) is satisfied at the PRECHARGE command time (T7) and that ^{t}RC (MIN) is satisfied at the next ACTIVATE command time (T18).
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 154: READ to PRECHARGE with 2tCK Preamble



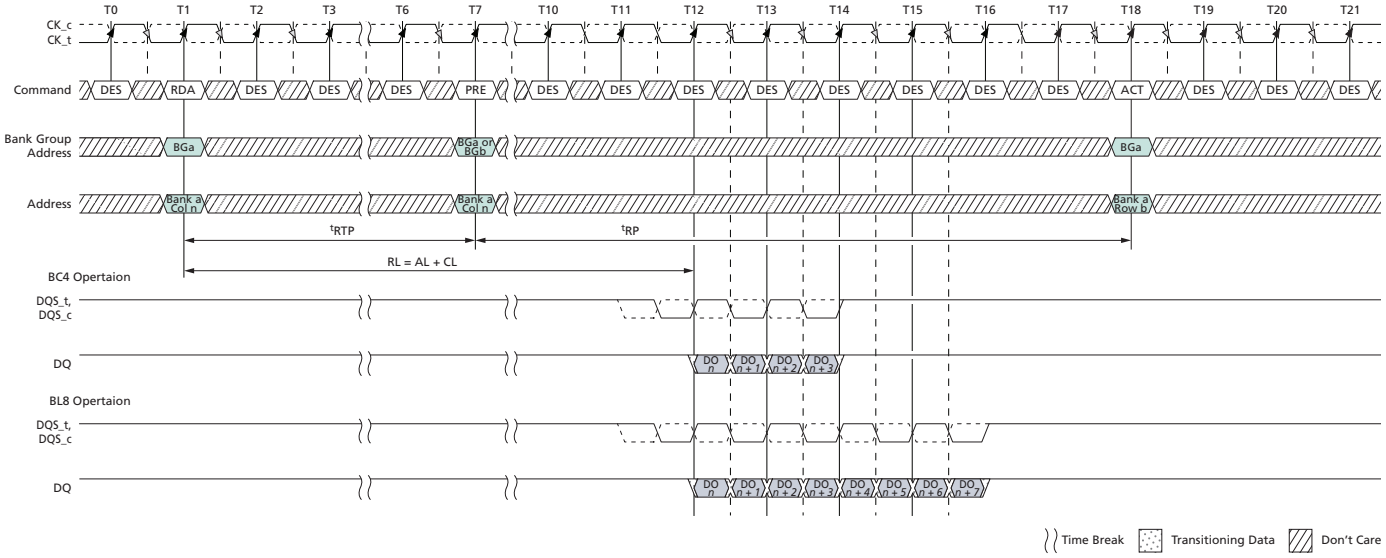
Notes: 1. RL = 11 (CL = 11, AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T7) and that tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 155: READ to PRECHARGE with Additive Latency and 1tCK Preamble



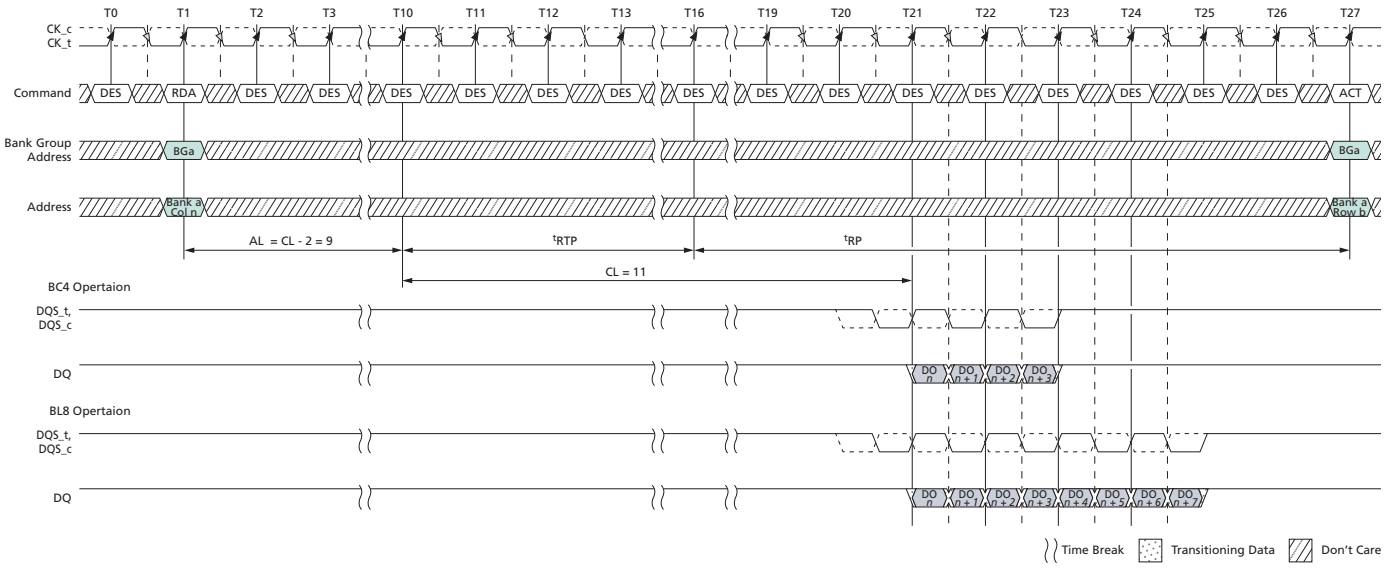
Notes: 1. RL =20 (CL = 11, AL = CL - 2), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T16) and that tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 156: READ with Auto Precharge and 1tCK Preamble



Notes: 1. RL = 11 (CL = 11, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001].
5. The example assumes that tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

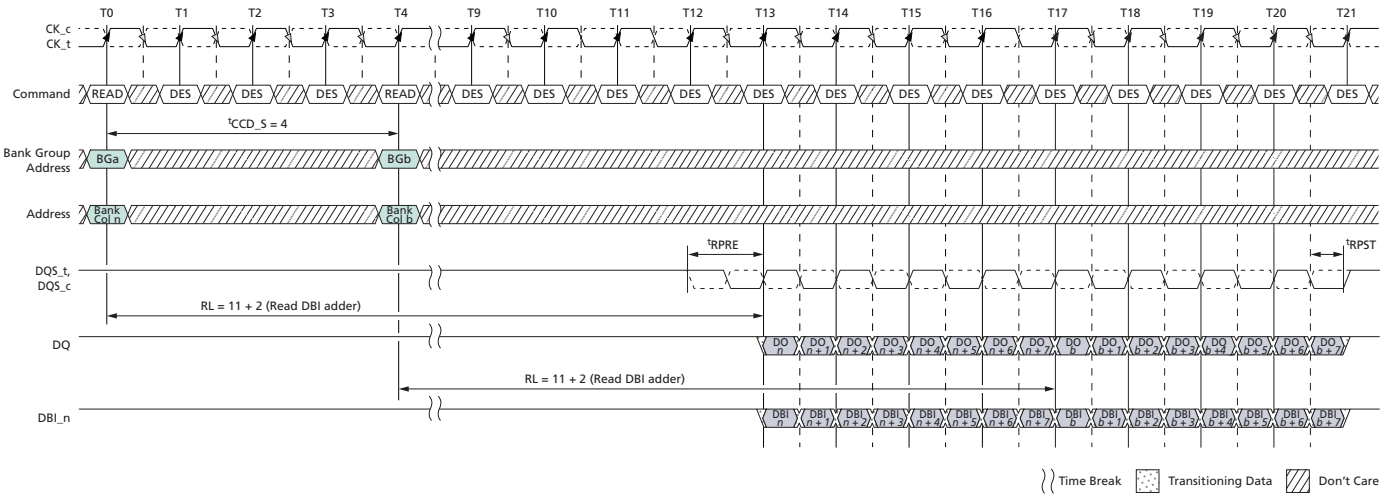
Figure 157: READ with Auto Precharge, Additive Latency, and 1tCK Preamble



Notes: 1. RL = 20 (CL = 11, AL = CL - 2), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[11:9] = 001.
5. The example assumes that tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Operation with Read Data Bus Inversion (DBI)

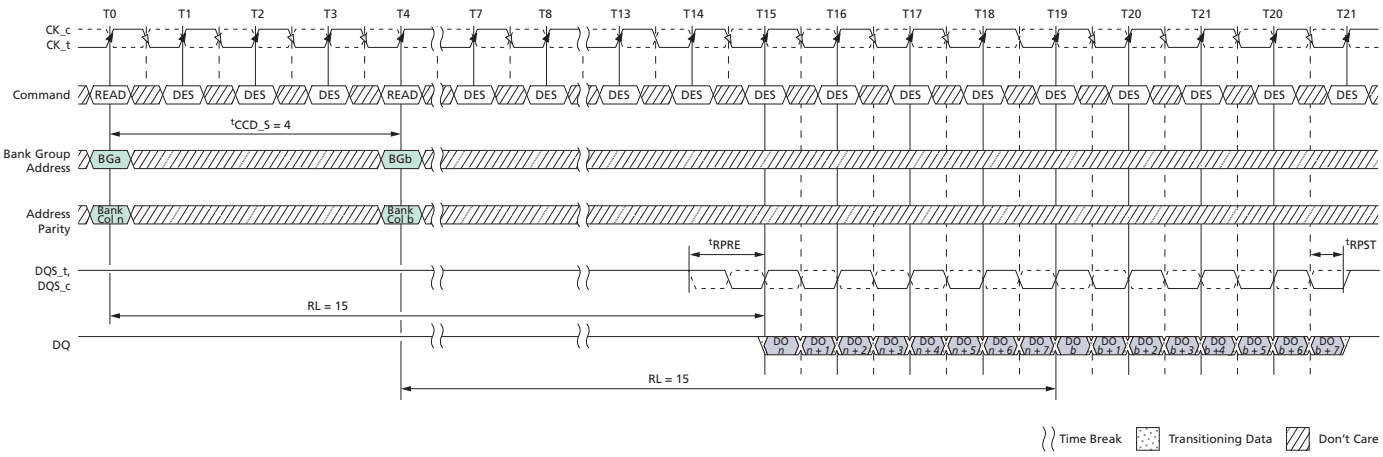
Figure 158: Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, RL = 11 + 2 (Read DBI adder).
2. DO *n* (or *b*) = data-out from column *n* (or *b*); DBI *n* (or *b*) = data bus inversion from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Enable.

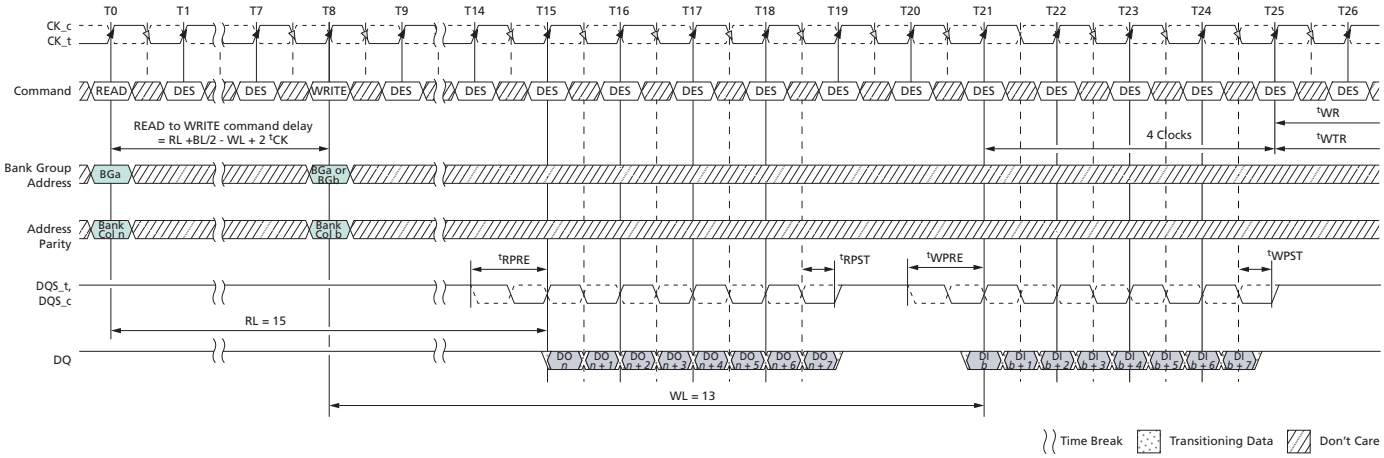
READ Operation with Command/Address Parity (CA Parity)

Figure 159: Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 01] and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable.

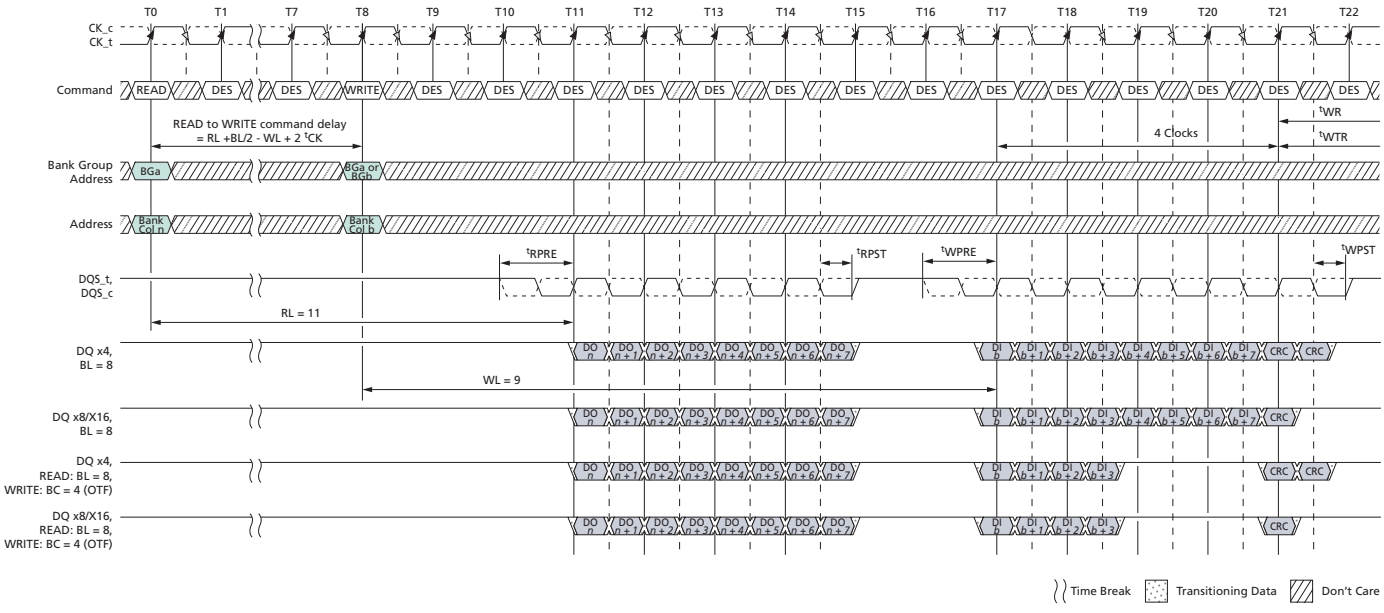
Figure 160: READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA Parity in Same or Different Bank Group



Notes: 1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), READ preamble = 1tCK, CWL = 9, AL = 0, PL = 4, (WL = CL + AL + PL = 13), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE command at T8.
5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ Followed by WRITE with CRC Enabled

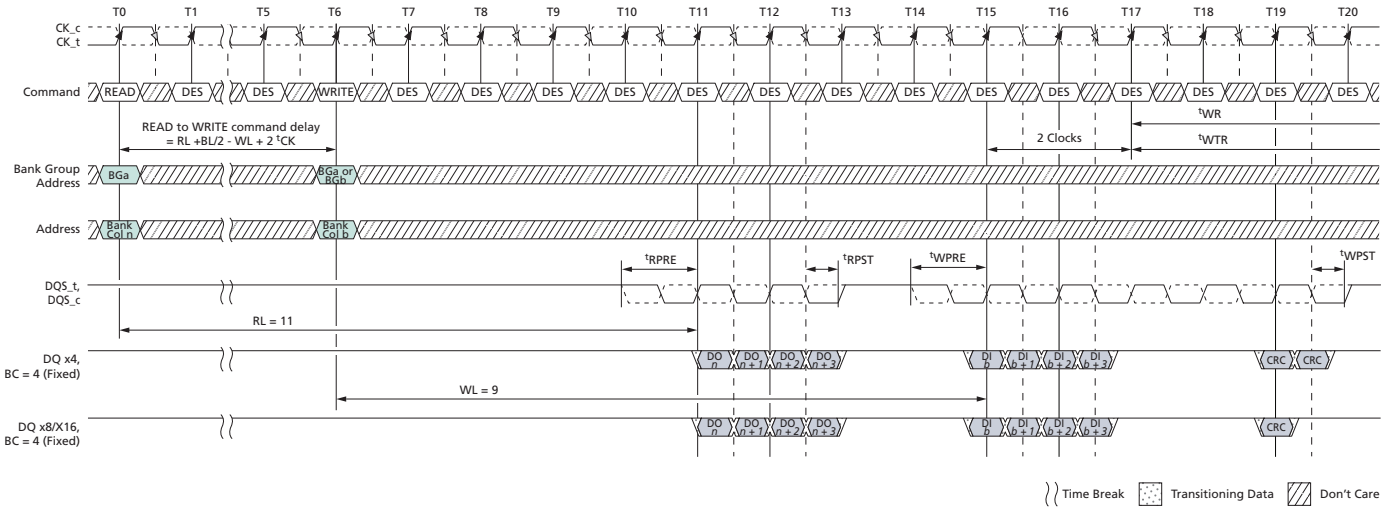
Figure 161: READ (BL8) to WRITE (BL8 or BC4: OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Notes: 1. BL = 8 (or BC = 4: OTF for Write), RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.

3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

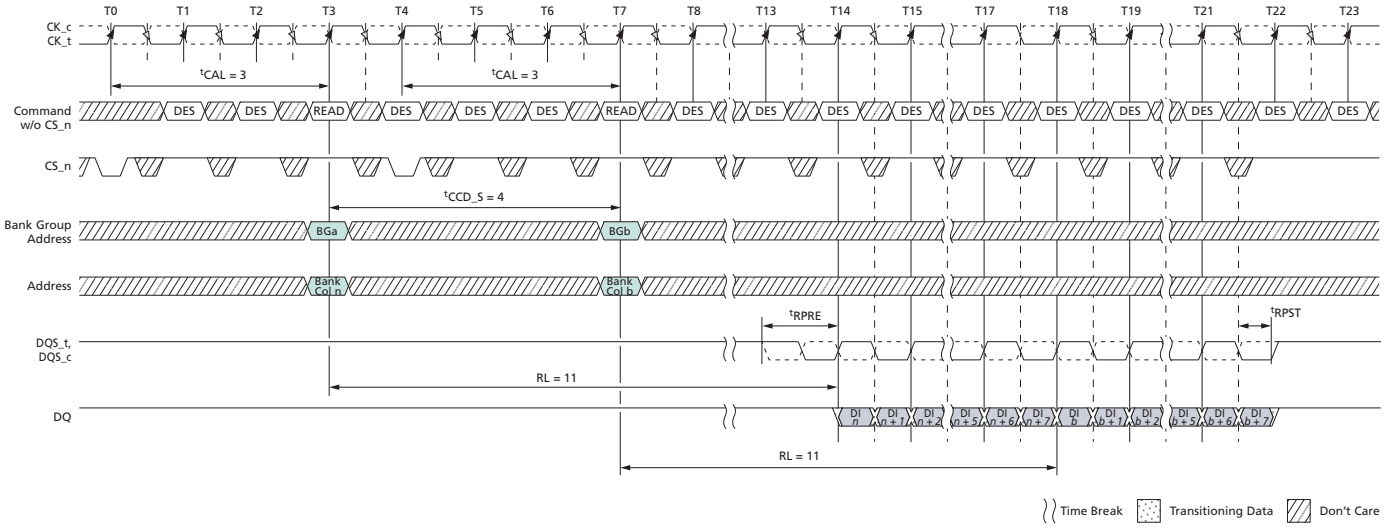
Figure 162: READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Notes: 1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

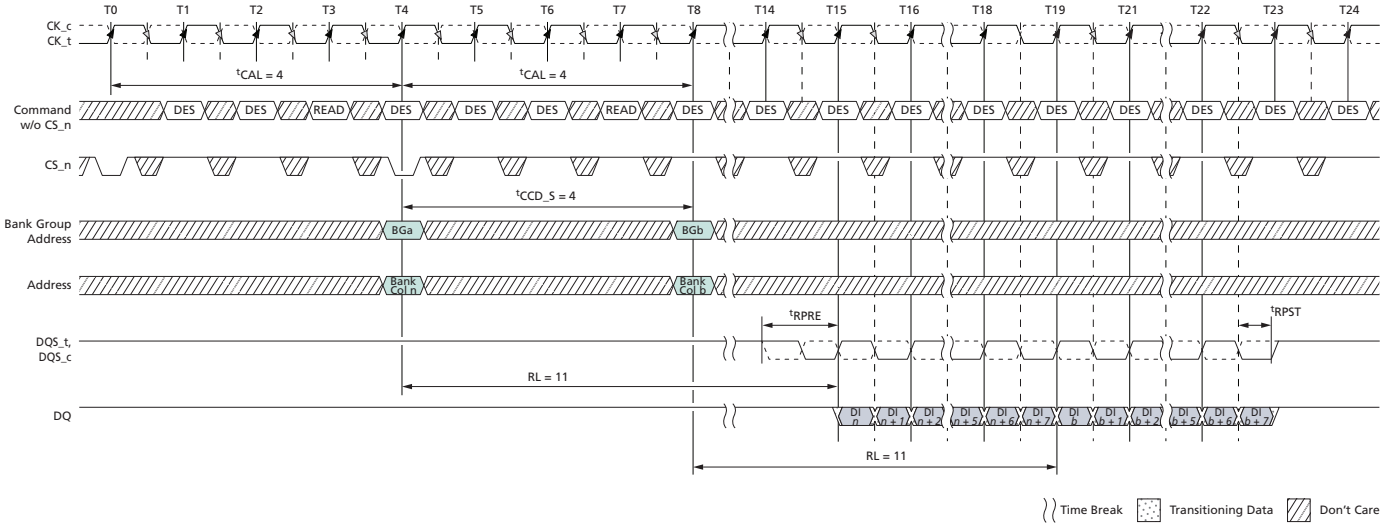
READ Operation with Command/Address Latency (CAL) Enabled

Figure 163: Consecutive READ (BL8) with CAL (3tCK) and 1tCK Preamble in Different Bank Group



Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T7.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

Figure 164: Consecutive READ (BL8) with CAL (4tCK) and 1tCK Preamble in Different Bank Group



Notes: 1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T8.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

WRITE Operation

Write Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Write Timing – Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship is shown below and is applicable in normal operation mode, that is, when the DLL is enabled and locked.

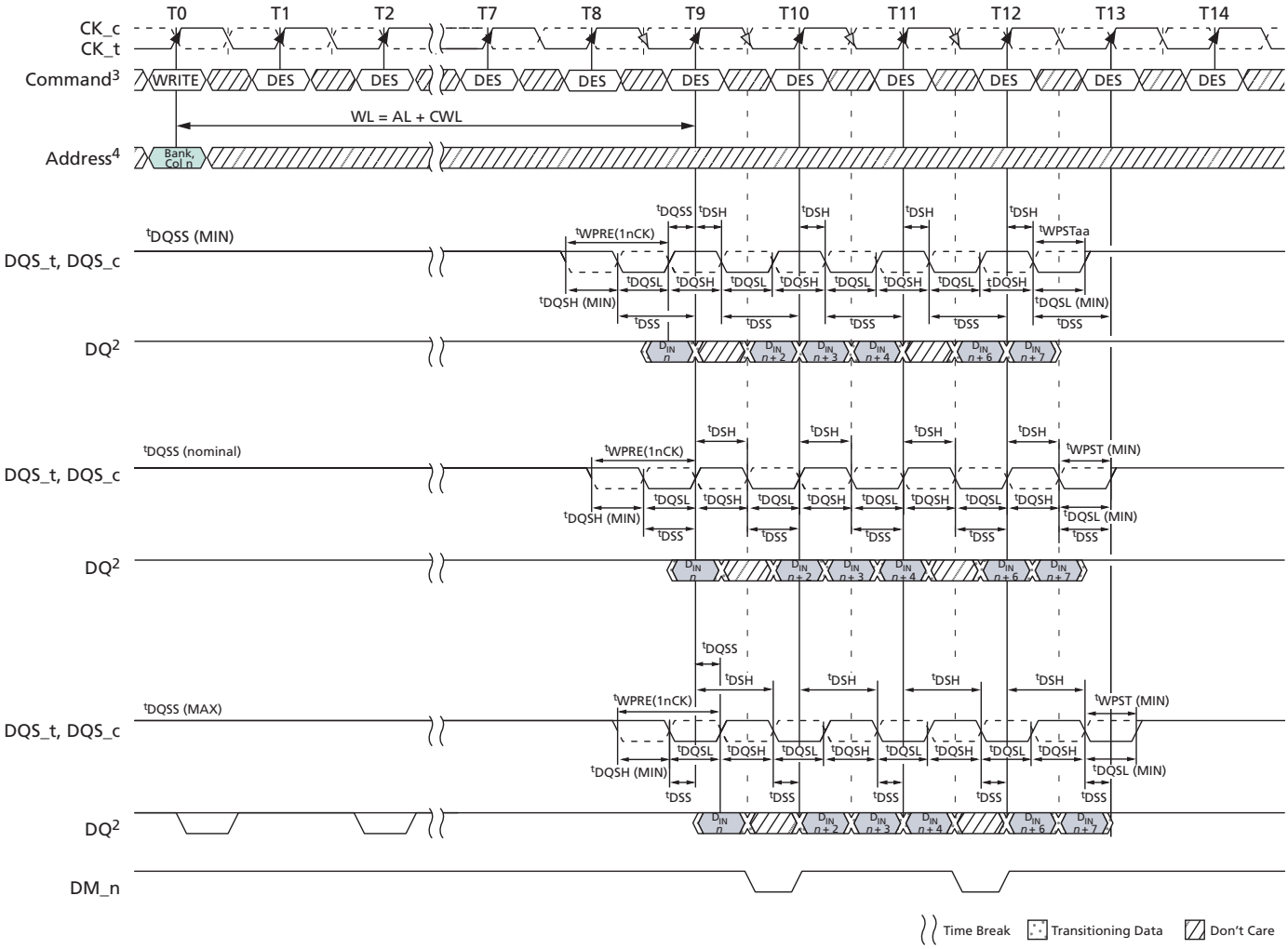
Rising data strobe edge parameters:

- ^{t}DQSS (MIN) to ^{t}DQSS (MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSS is the actual position of a rising strobe edge relative to CK.
- ^{t}DQSH describes the data strobe high pulse width.
- ^{t}WPST strobe going to HIGH, nondrive level (shown in the postamble section of the graphic below).

Falling data strobe edge parameters:

- ^{t}DQSL describes the data strobe low pulse width.
- ^{t}WPRE strobe going to LOW, initial drive level (shown in the preamble section of the graphic below).

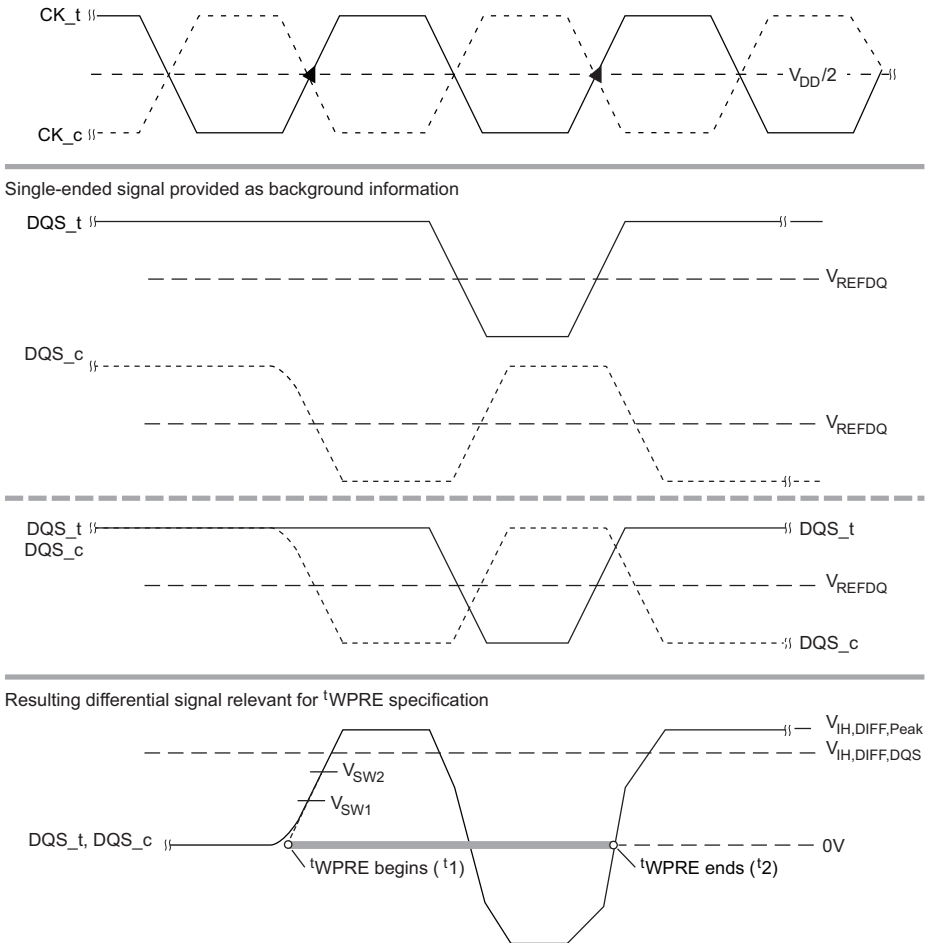
Figure 165: Write Timing Definition



Notes: 1. BL8, WL = 9 (AL = 0, CWL = 9).
2. D_{IN} *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. ^{t}DQSS must be met at each rising clock edge.

tWPRE Calculation

Figure 166: tWPRE Method for Calculating Transitions and Endpoints



Notes: 1. $V_{sw1} = (0.1) \times V_{IH,diff,DQS}$.
2. $V_{sw2} = (0.9) \times V_{IH,diff,DQS}$.