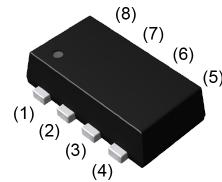


V_{DSS}	-12V
$R_{DS(on)}$ (Max.)	43mΩ
I_D	±3.5A
P_D	1.25W

●Outline

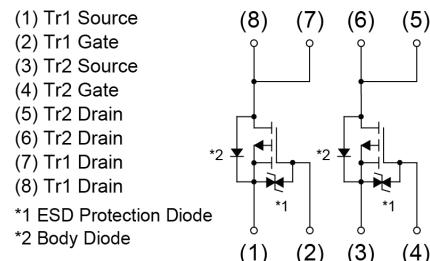
TSST8



●Features

- 1) Low on - resistance.
- 2) -1.5V Drive.
- 3) Built-in G-S Protection Diode.
- 4) Small Surface Mount Package (TSST8).
- 5) Pb-free lead plating ; RoHS compliant

●Inner circuit



●Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	8
	Basic ordering unit (pcs)	3000
	Taping code	TR
	Marking	J11

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$) <It is the same ratings for the Tr1 and Tr2>

Parameter	Symbol	Value	Unit
Drain - Source voltage	V_{DSS}	-12	V
Continuous drain current	I_D	±3.5	A
Pulsed drain current	$I_{D,pulse}^{*1}$	±12	A
Gate - Source voltage	V_{GSS}	0 ~ -8	V
Power dissipation	total	P_D^{*2}	1.25
	element		1
	total	P_D^{*3}	0.6
Junction temperature	T_j	150	°C
Range of storage temperature	T_{stg}	-55 to +150	°C

● Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	total	R_{thJA}^{*2}	-	-	100
	element		-	-	125
	total	R_{thJA}^{*3}	-	-	208

● Electrical characteristics ($T_a = 25^\circ\text{C}$) <It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -1\text{mA}$	-12	-	-	V
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	$I_D = -1\text{mA}$ referenced to 25°C	-	-5.0	-	$\text{mV}/^\circ\text{C}$
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}$	-	-	-10	μA
Gate - Source leakage current	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = -8\text{V}$	-	-	-10	μA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = -6\text{V}, I_D = -1\text{mA}$	-0.3	-	-1.0	V
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	$I_D = -1\text{mA}$ referenced to 25°C	-	2.7	-	$\text{mV}/^\circ\text{C}$
Static drain - source on - state resistance	$R_{DS(on)}^{*4}$	$V_{GS} = -4.5\text{V}, I_D = -3.5\text{A}$	-	31	43	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -1.7\text{A}$	-	43	60	
		$V_{GS} = -1.8\text{V}, I_D = -1.7\text{A}$	-	60	90	
		$V_{GS} = -1.5\text{V}, I_D = -0.7\text{A}$	-	80	160	
Gate input resistance	R_G	$f = 1\text{MHz}, \text{open drain}$	-	10	-	Ω
Forward Transfer Admittance	$ Y_{fs} ^{*4}$	$V_{DS} = -6\text{V}, I_D = -3.5\text{A}$	4	-	-	S

●Electrical characteristics ($T_a = 25^\circ\text{C}$) <It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	$V_{GS} = 0\text{V}$ $V_{DS} = -6\text{V}$ $f = 1\text{MHz}$	-	2600	-	pF
Output capacitance	C_{oss}		-	200	-	
Reverse transfer capacitance	C_{rss}		-	190	-	
Turn - on delay time	$t_{d(on)}^{\ast 4}$	$V_{DD} \approx -6\text{V}, V_{GS} = -4.5\text{V}$ $I_D = -1.7\text{A}$ $R_L = 3.5\Omega$ $R_G = 10\Omega$	-	15	-	ns
Rise time	$t_r^{\ast 4}$		-	30	-	
Turn - off delay time	$t_{d(off)}^{\ast 4}$		-	170	-	
Fall time	$t_f^{\ast 4}$		-	60	-	

●Gate charge characteristics ($T_a = 25^\circ\text{C}$) <It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Total gate charge	$Q_g^{\ast 4}$	$V_{DD} \approx -6\text{V}$ $I_D = -3.5\text{A}$ $V_{GS} = -4.5\text{V}$	-	22	-	nC
Gate - Source charge	$Q_{gs}^{\ast 4}$		-	3.9	-	
Gate - Drain charge	$Q_{gd}^{\ast 4}$		-	3.1	-	

●Body diode electrical characteristics (Source-Drain) ($T_a = 25^\circ\text{C}$)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous forward current	I_S	$T_a = 25^\circ\text{C}$	-	-	-0.8	A
Body diode pulse current	$I_{SP}^{\ast 1}$		-	-	-12	
Forward voltage	$V_{SD}^{\ast 4}$	$V_{GS} = 0\text{V}, I_S = -3.5\text{A}$	-	-	-1.2	V

*1 $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board (30×30×0.8mm)

*3 Mounted on a FR4 (20×20×0.8mm)

*4 Pulsed

●Electrical characteristic curves

Fig.1 Power Dissipation Derating Curve

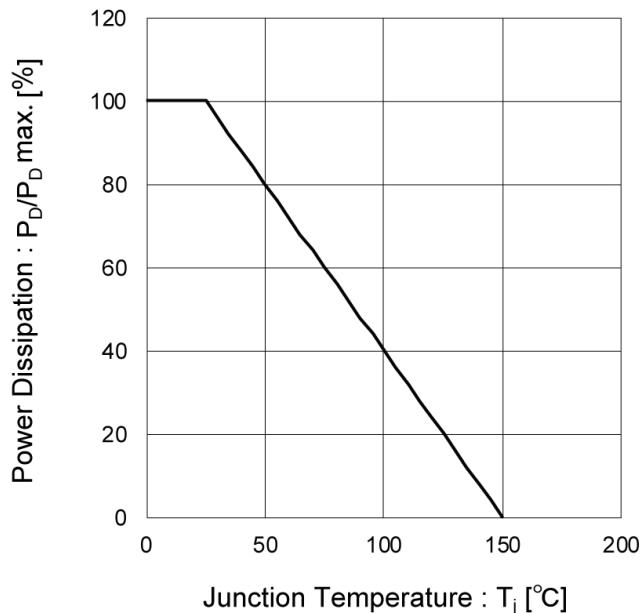


Fig.2 Maximum Safe Operating Area

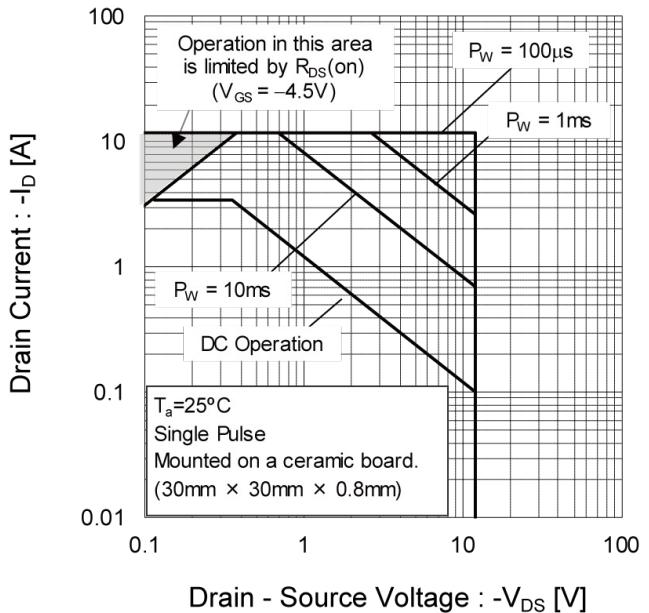


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

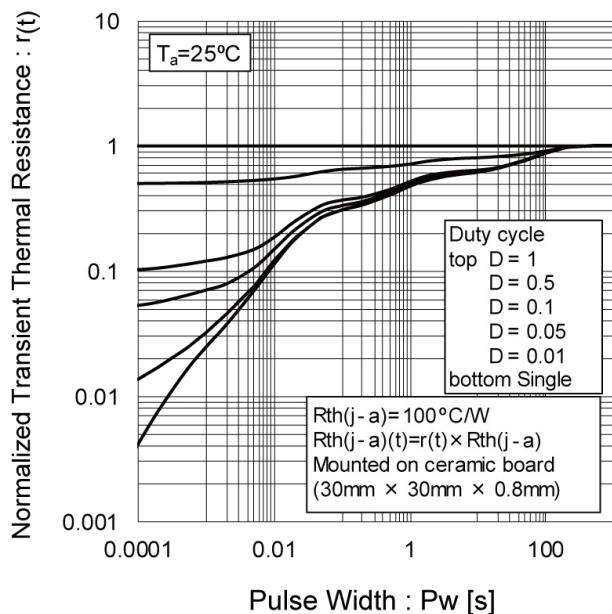
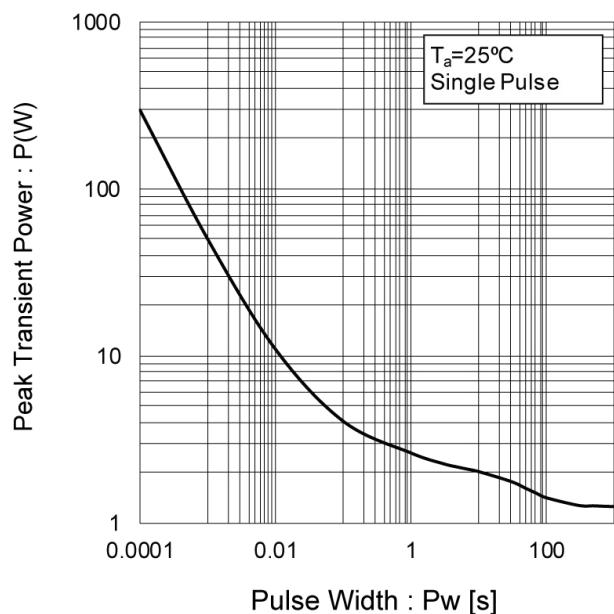


Fig.4 Single Pulse Maximum Power dissipation



●Electrical characteristic curves

Fig.5 Typical Output Characteristics(I)

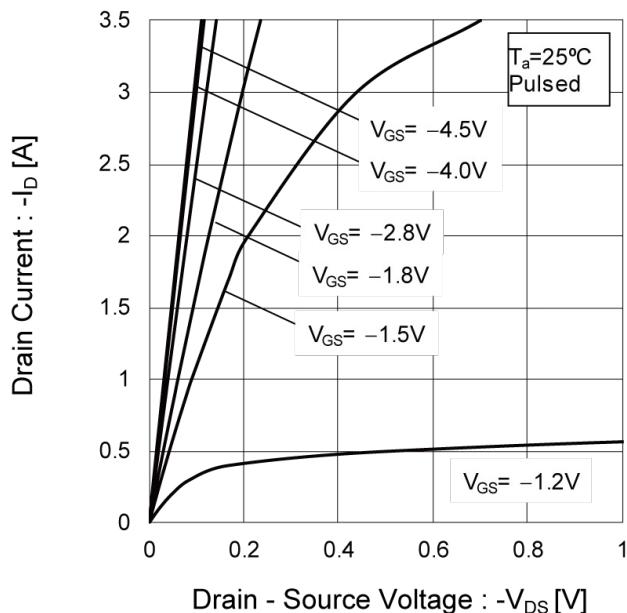


Fig.6 Typical Output Characteristics(II)

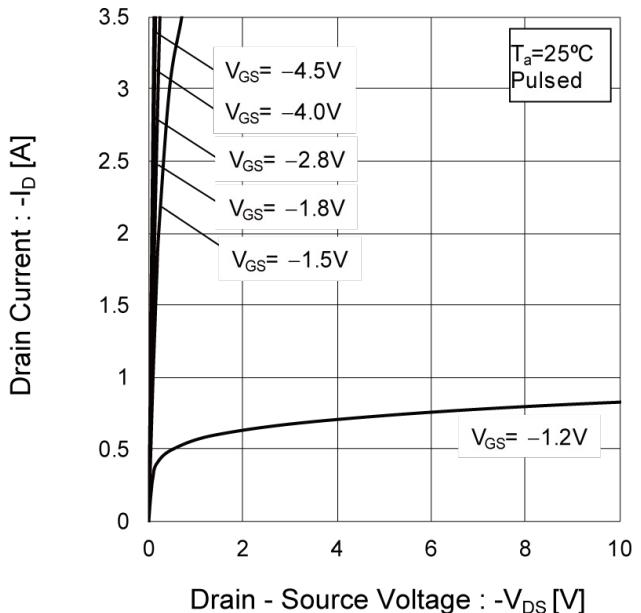
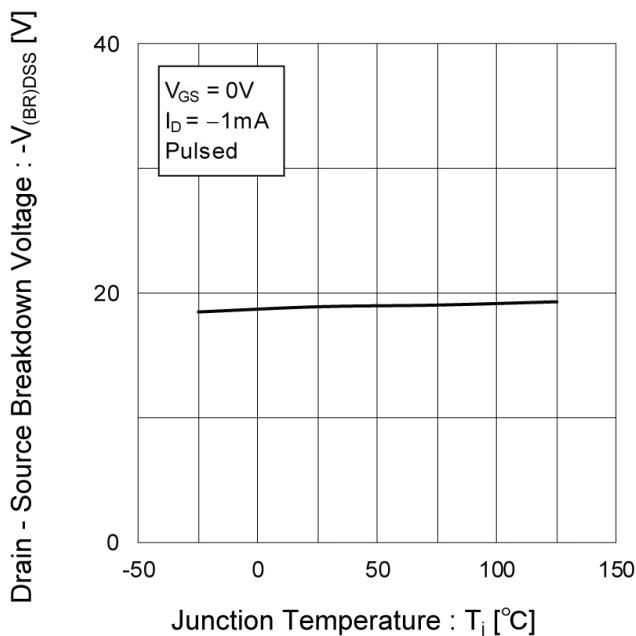
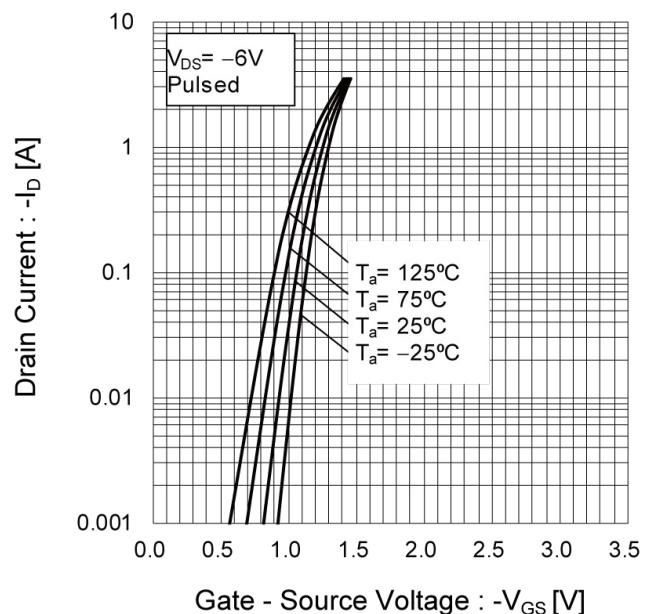
Fig.7 Breakdown Voltage vs.
Junction Temperature

Fig.8 Typical Transfer Characteristics



●Electrical characteristic curves

Fig.9 Gate Threshold Voltage vs.
Junction Temperature

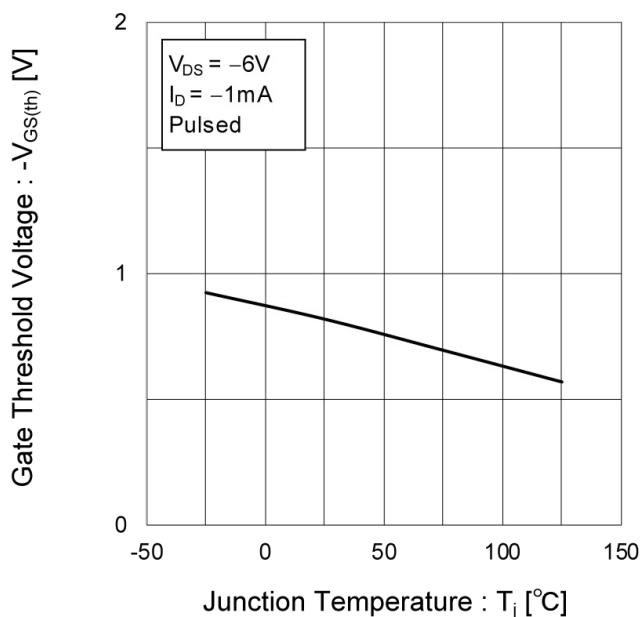


Fig.10 Forward Transfer Admittance vs.
Drain Current

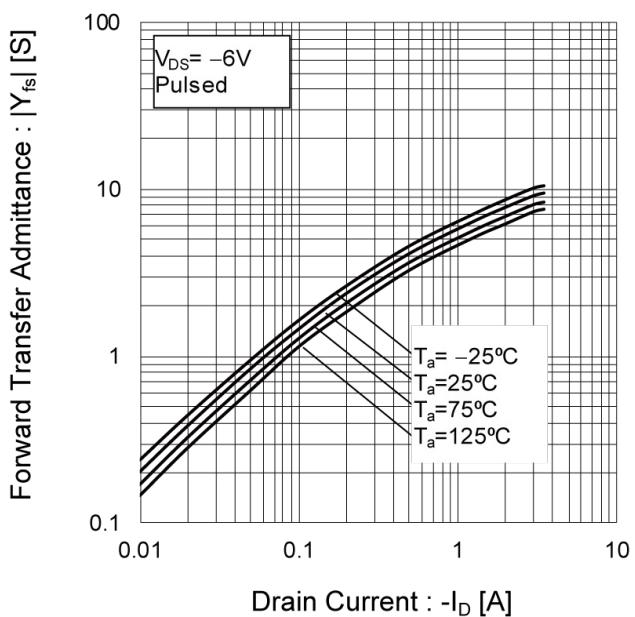


Fig.11 Drain Current Derating Curve

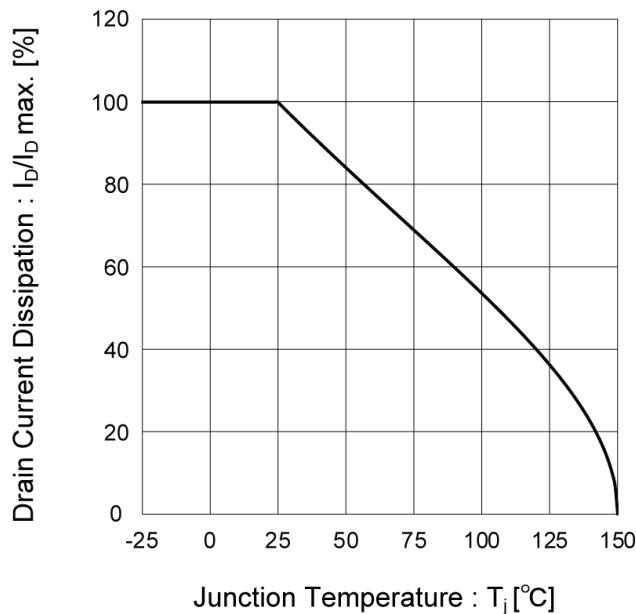
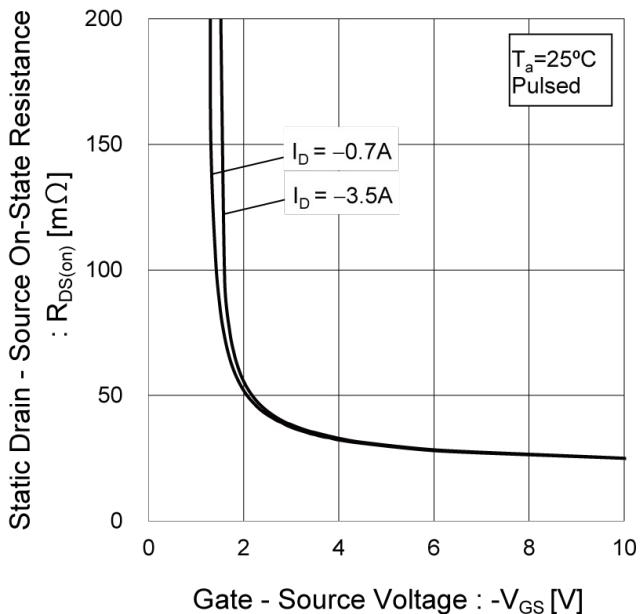


Fig.12 Static Drain - Source On - State
Resistance vs. Gate Source Voltage



● Electrical characteristic curves

Fig.13 Static Drain - Source On - State
Resistance vs. Junction Temperature

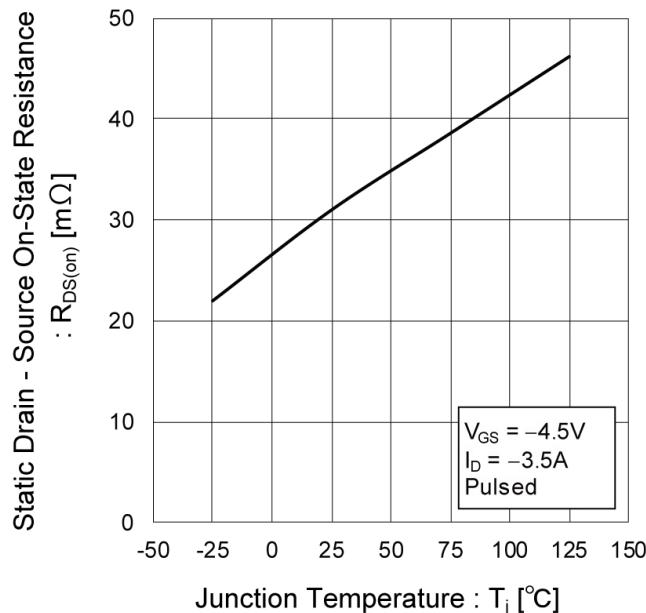
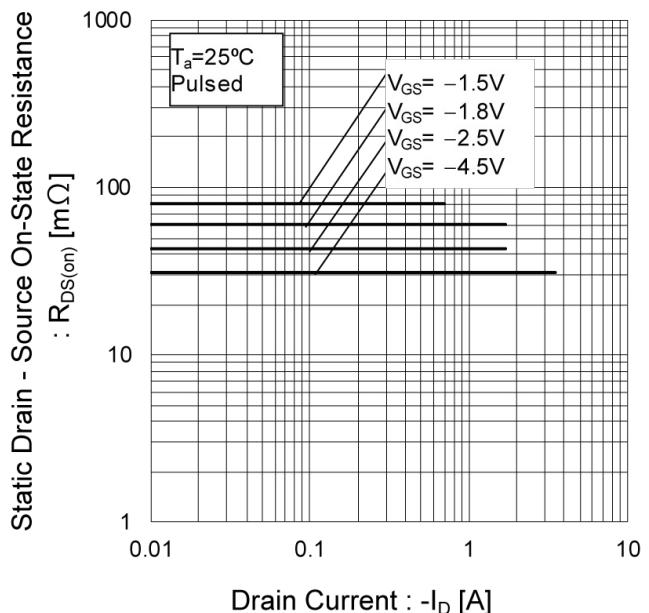


Fig.14 Static Drain - Source On - State
Resistance vs. Drain Current(I_D)



●Electrical characteristic curves

Fig.15 Static Drain - Source On - State
Resistance vs. Drain Current(II)

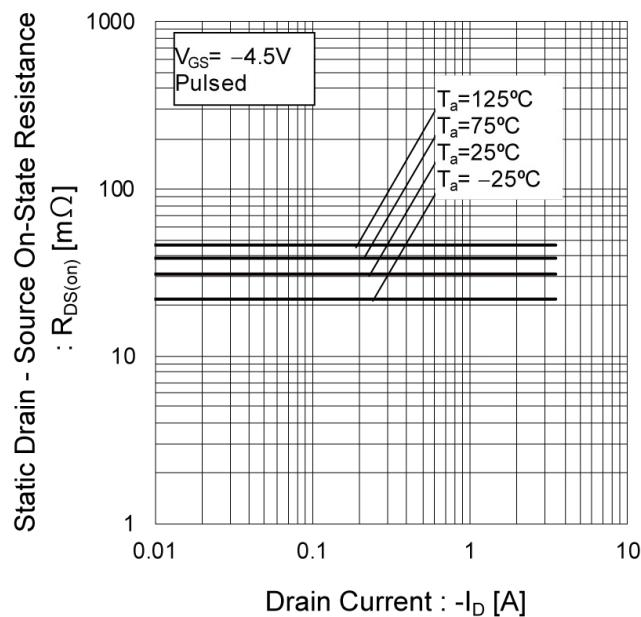


Fig.16 Static Drain - Source On - State
Resistance vs. Drain Current(III)

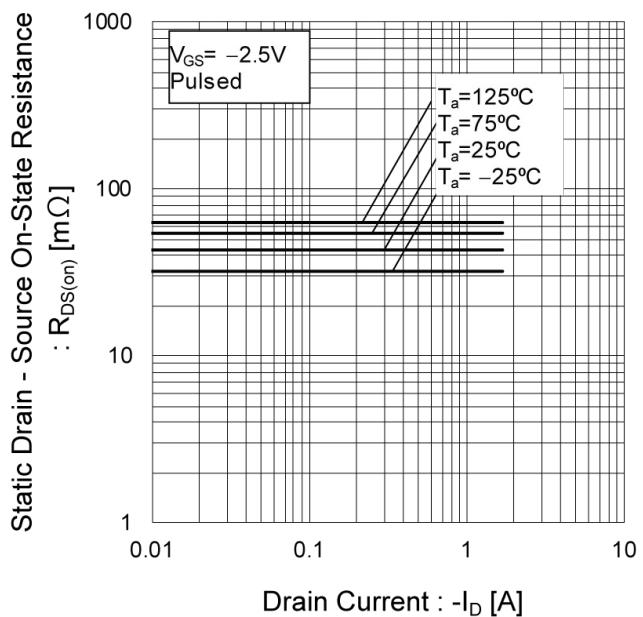


Fig.17 Static Drain - Source On - State
Resistance vs. Drain Current(IV)

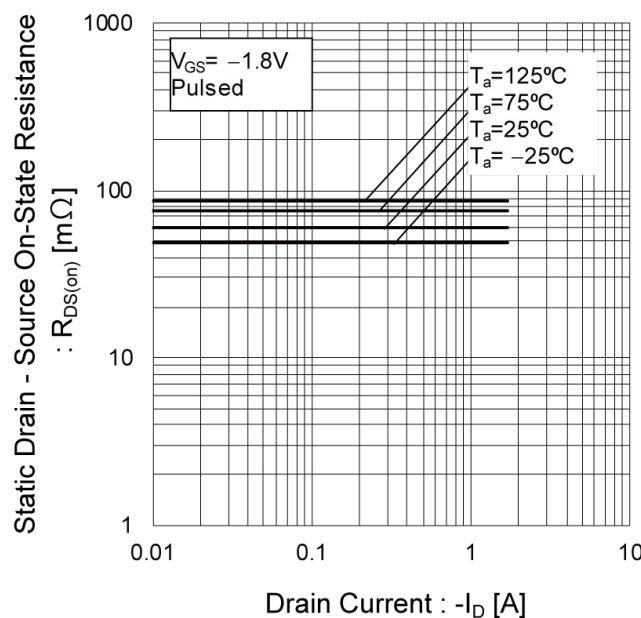
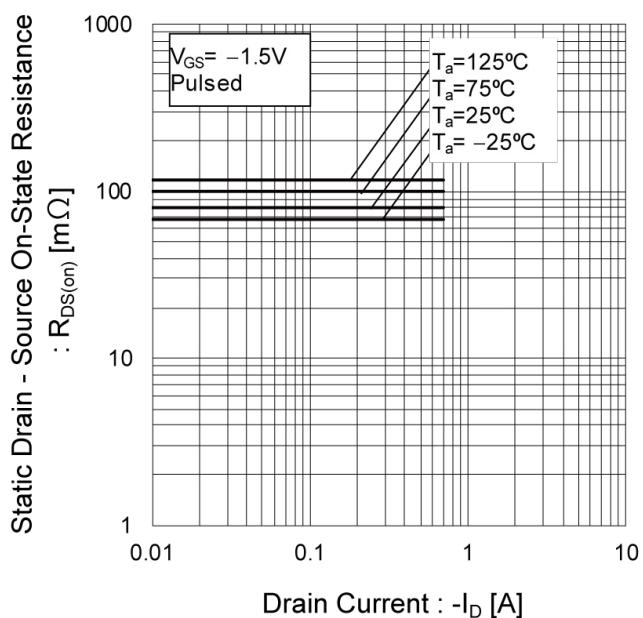


Fig.18 Static Drain - Source On - State
Resistance vs. Drain Current(V)



●Electrical characteristic curves

Fig.19 Typical Capacitance vs.
Drain - Source Voltage

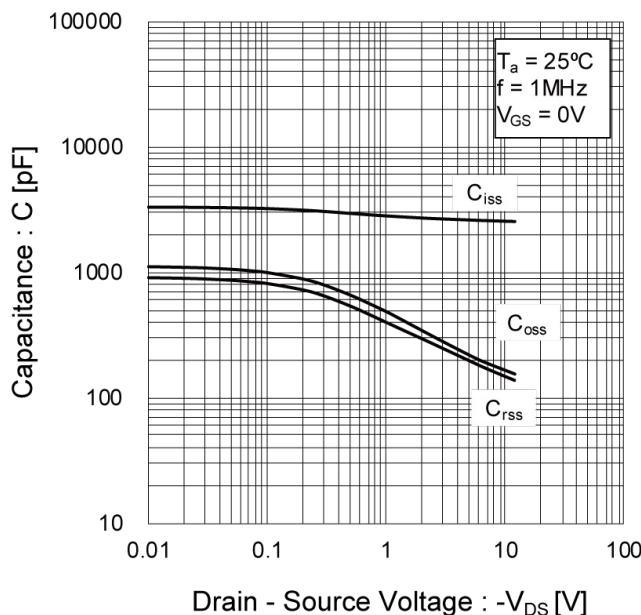


Fig.20 Switching Characteristics

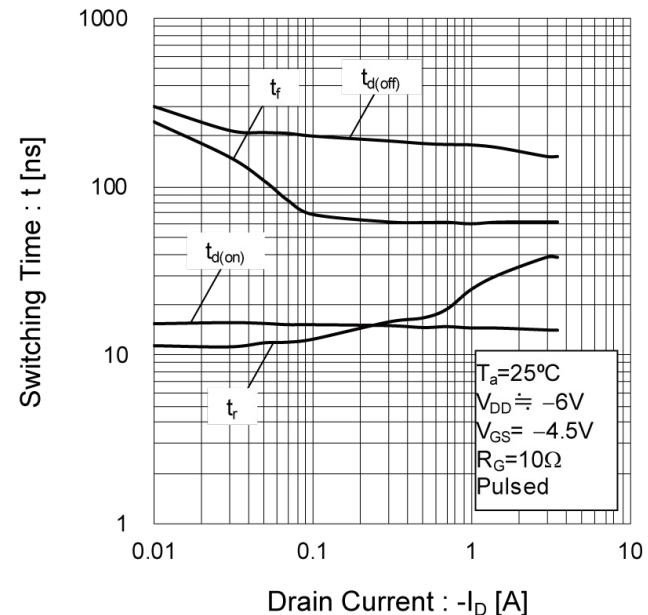


Fig.21 Dynamic Input Characteristics

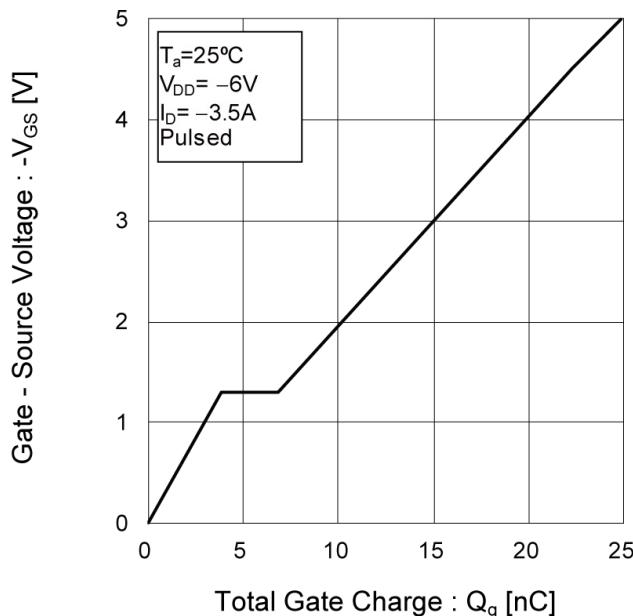
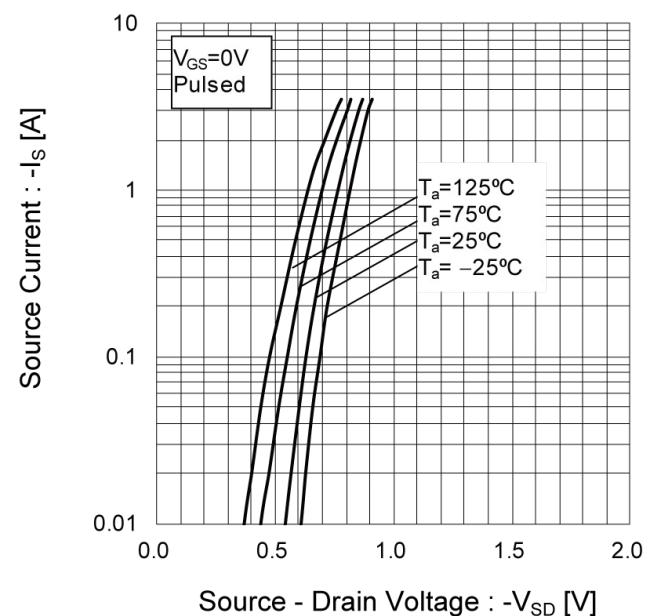


Fig.22 Source Current vs.
Source Drain Voltage



● **Measurement circuits <It is the same for the Tr1 and Tr2>**

Fig. 1-1 SWITCHING TIME MEASUREMENT CIRCUIT

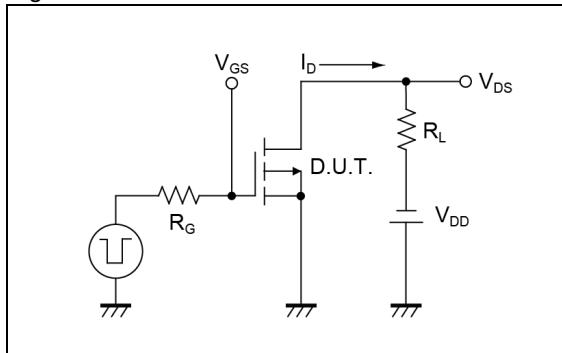


Fig. 1-2 SWITCHING WAVEFORMS

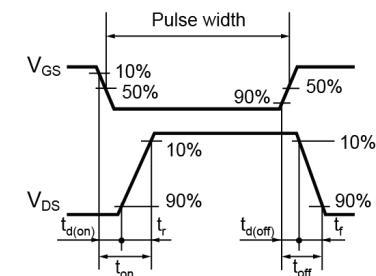


Fig. 2-1 GATE CHARGE MEASUREMENT CIRCUIT

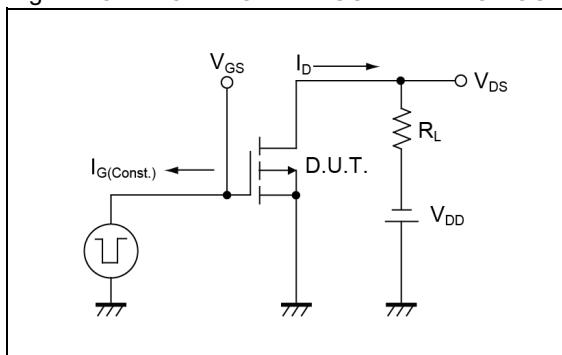
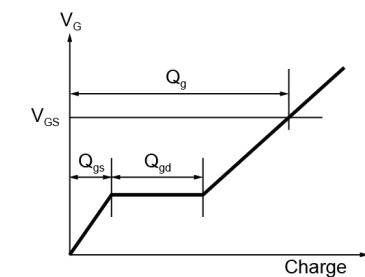


Fig. 2-2 GATE CHARGE WAVEFORM

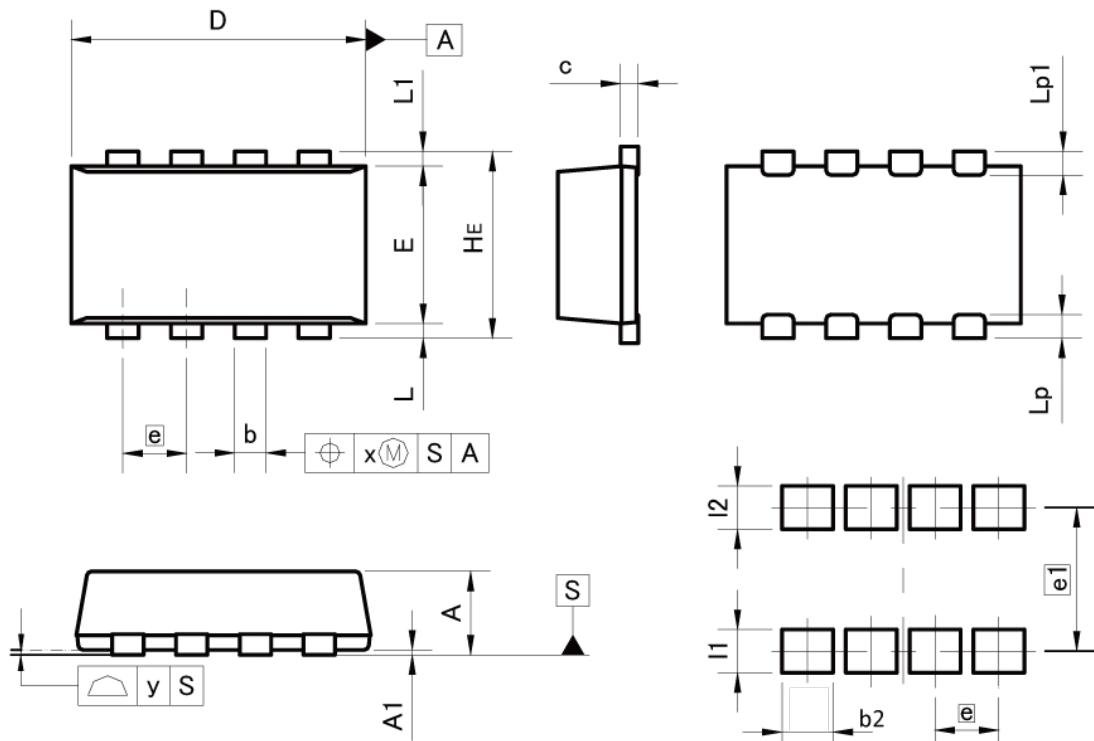


● **Notice**

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

●Dimensions

TSST8



Pattern of terminal position areas
[Not a pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.85	0.030	0.033
A1	0.00	0.05	0.000	0.002
b	0.22	0.42	0.009	0.017
c	0.12	0.22	0.005	0.009
D	2.90	3.10	0.114	0.122
E	1.50	1.70	0.059	0.067
e	0.65		0.026	
HE	1.80	2.00	0.071	0.079
L	0.05	0.25	0.002	0.010
L1	0.05	0.25	0.002	0.010
Lp	0.15	0.34	0.006	0.013
Lp1	0.15	0.34	0.006	0.013
x	—	0.10	—	0.004
y	—	0.10	—	0.004

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b2	—	0.52	—	0.020
e1	1.46		0.057	
I1	—	0.44	—	0.017
I2	—	0.44	—	0.017

Dimension in mm/inches

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