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March 2009

# FDS6675BZ

# P-Channel PowerTrench® MOSFET

-30V, -11A, 13mΩ

## **General Description**

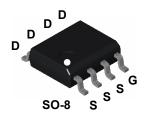
This P-Channel MOSFET is producted using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance.

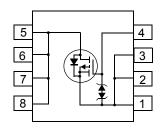
This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.



### **Features**

- Max  $r_{DS(on)} = 13m\Omega$  at  $V_{GS} = -10V$ ,  $I_D = -11A$
- Max  $r_{DS(on)}$  = 21.8m $\Omega$  at  $V_{GS}$  = -4.5V,  $I_D$  = -9A
- Extended V<sub>GS</sub> range (-25V) for battery applications
- HBM ESD protection level of 5.4 KV typical (note 3)
- High performance trench technology for extremely low rDS(on)
- High power and current handing capability
- RoHS Compliant





# MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
$V_{DS}$	Drain to Source Voltage		-30	V
$V_{GS}$	Gate to Source Voltage		±25	V
ı	Drain Current -Continuous	(Note 1a)	-11	۸
ID	-Pulsed		-55	Α
	Power Dissipation for Single Operation	(Note 1a)	2.5	
$P_{D}$		(Note 1b)	1.2	W
		(Note 1c)	1.0	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to 150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

## **Package Marking and Ordering Information**

	Device Marking	Device	Reel Size	Tape Width	Quantity
Ì	FDS6675BZ	FDS6675BZ	13"	12mm	2500 units

# Electrical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = -250μA, referenced to 25°C		-20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$			-1	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS}$ = ±25V, $V_{DS}$ = 0V			±10	μΑ

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1	-2	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25°C		15.7		mV/°C
r Drain to Source On Resistance	V <sub>GS</sub> = -10V , I <sub>D</sub> = -11A		10.8	13.0		
	Drain to Source On Resistance	$V_{GS} = -4.5V$ , $I_{D} = -9A$		17.4	21.8	mΩ
r <sub>DS(on)</sub>	Brain to course on registance	$V_{GS} = -10V, I_D = -11A$ $T_J = 125^{\circ}C$		15.0	18.8	11122
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5V$ , $I_{D} = -11A$		34		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 45\\ \\ - 0\\	1855	2470	pF
Coss	Output Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz	335	450	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	11111112	330	500	pF

### **Switching Characteristics (Note 2)**

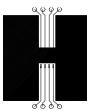
t <sub>d(on)</sub>	Turn-On Delay Time		3.0	10	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = -15V, $I_{D}$ = -11A $V_{GS}$ = -10V, $R_{GS}$ = 6 $\Omega$	7.8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -10V, K <sub>GS</sub> = 012	120	200	ns
t <sub>f</sub>	Fall Time		60	100	ns
Qg	Total Gate Charge	$V_{DS} = -15V, V_{GS} = -10V,$ $I_{D} = -11A$	44	62	nC
$Q_g$	Total Gate Charge	V 45V.V 5V	25	35	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = -15V, V_{GS} = -5V,$ $I_{D} = -11A$	7.2		nC
Q <sub>gd</sub>	Gate to Drain Charge	D = -11A	11.4		nC

#### **Drain-Source Diode Characteristics**

,	$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = -2.1A$	-0.7	-1.2	V
1	t <sub>rr</sub>	Reverse Recovery Time	$I_F = -11A$ , di/dt = 100A/ $\mu$ s		42	ns
(	Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = -11A, di/dt = 100A/μs		30	nC

#### Notes

1. R<sub>8,IA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>8,IC</sub> is guaranteed by design while R<sub>8,CA</sub> is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

- Scale 1:1 on letter size paper
- 2: Pulse Test:Pulse Width <300 us, Duty Cycle < 2.0%
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

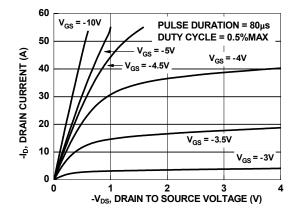


Figure 1. On Region Characteristics

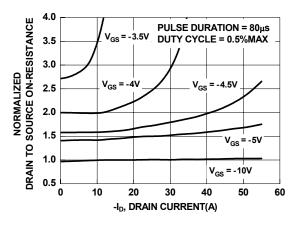


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

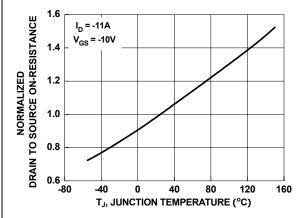


Figure 3. Normalized On Resistance vs Junction Temperature

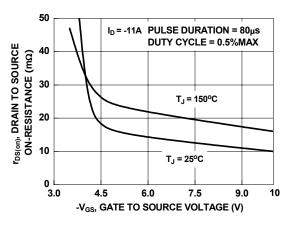


Figure 4. On-Resistance vs Gate to Source Voltage

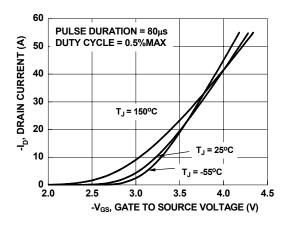


Figure 5. Transfer Characteristics

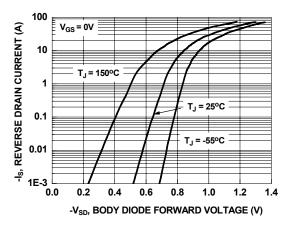
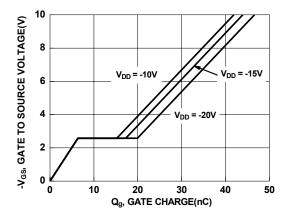


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted



4000 C<sub>iss</sub>

1000 C<sub>oss</sub>

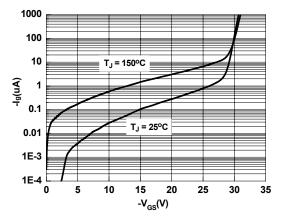
1000 C<sub>rss</sub>

100 C<sub>rss</sub>

100

Figure 7. Gate Charge Characteristics

Figure 8. Capacitance vs Drain to Source Voltage



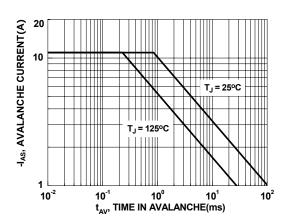
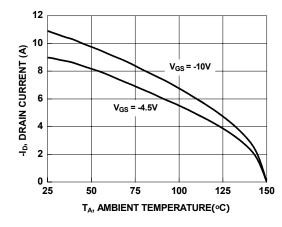


Figure 9.  $I_g vs V_{GS}$ 

Figure 10. Unclamped Inductive Switching Capability



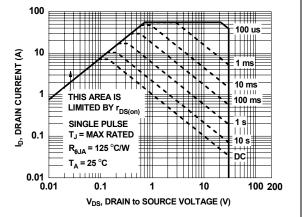


Figure 11. Maximum Continuous Drain Current vs
Ambient Temperature

Figure 12. Forward Bias Safe Operating Area



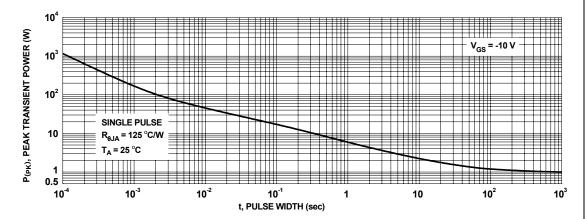


Figure 13. Single Pulse Maximum Power Dissipation

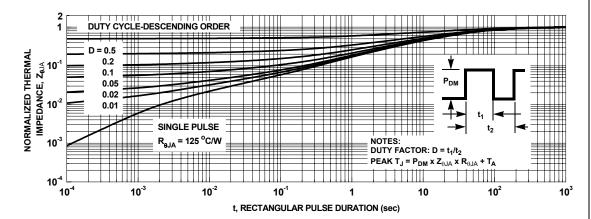


Figure 14. Junction-to-Ambient Transient Thermal Response Curve





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