

M5480

LED DISPLAY DRIVER

FEATURES SUMMARY

- 3 1/2 DIGIT LED DRIVER (23 segments)
- CURRENT GENERATOR OUTPUTS (no resistors required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application Examples:

- MICROPROCESSOR DISPLAY
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

Figure 1. Package



DESCRIPTION

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a C 1/2 digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected sittler to V_{DD} or to a separate supply of 1.3.2.4 maximum.

The M5480 is a pin-p-pin replacement of the NS MM 5480.

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Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage	– 0.3 to 15	V
VI	Input Voltage	– 0.3 to 15	V
V _{O(off)}	Off State Output Voltage	15	V
Ι _Ο	Output Sink Current	40	mA
P _{TOT}	Total Package Power Dissipation at 25°C	940	mW
101	Total Package Power Dissipation at 85°C	490	mW
Тj	Junction Temperature	150	°C
T _{OP}	Operating Temperature Range	– 25 to 85	°C
T _{STG}	Storage Temperature Range	– 65 to 150	°C

Table 1. Absolute Maximum Ratings

Note: Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Static Electrical Characteristics

(T _{amb} wit	hin operating range	Vpp = 4.75V to	$13.2V, V_{SS} = 0V$, unless otherwise	specified)
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Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Supply Voltage.,75		5		13.2	V
Supply Current	V _{DD} = 13.2V			7	mA
Input Voltage Logical "0" Level	± 10µA Input Bias	- 0.3		0.08	V
Logical "1" Level	$4.75 \le V_{DD} \le 5.25$	2.2		V_{DD}	V
	V _{DD} > 5.25	V _{DD} - 2		V_{DD}	V
Brightness Input Current (note 2)		0		0.75	mA
Brightness Input Voltage (pin 13)	Input Current = 750μ A, T _{amb} = 25° C	3		4.3	V
Off State Out. Voltage			13.2	18	V
Out. Sink Current (note 3)	6				
Segment OFF	$V_{O} = 3V$			10	μA
Segment ON	$V_{O} = 1V$ (note 4)				
	Brightness In. = $0\mu A$	0		10	μA
	Brightness In. = 100μA	2	2,7	4	mA
	Brightness In. = 750µA	12	15	25	mA
Input Clock Frequency		0		0.5	MHz
Output Matching (note 1)				± 20	%
	Supply Voltage.,75 Supply Current Input Voltage Logical "0" Level Logical "1" Level Brightness Input Current (note 2) Brightness Input Voltage (pin 13) Off State Out. Voltage Out. Sink Current (note 3) Segment OFF Segment ON	Supply Voltage.,75VSupply Current $V_{DD} = 13.2V$ Input Voltage Logical "0" Level Logical "1" Level $\pm 10\mu A$ Input Bias $4.75 \le V_{DD} \le 5.25$ $V_{DD} > 5.25$ Brightness Input Current (note 2)Input Current = 750 μA , Tamb = 25°CBrightness Input VoltageInput Current = 750 μA , Tamb = 25°COff State Out. Voltage $V_O = 3V$ $V_O = 1V$ (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA Input Clock FrequencyInput Clock Frequency	Supply Voltage.,75VDD = 13.2VSupply Current $V_{DD} = 13.2V$ Input Voltage Logical "0" Level $\pm 10\mu$ A Input Bias- 0.3Logical "1" Level $4.75 \le V_{DD} \le 5.25$ 2.2 $V_{DD} > 5.25$ $V_{DD} - 2$ Brightness Input Current (note 2)0Brightness Input Voltage (pin 13)Input Current = 750 μ A, Tamb = 25°C3Off State Out. VoltageVO = 3VSegment OFFVO = 1V (note 4)Segment ONBrightness In. = 0 μ A0Brightness In. = 100 μ A2Brightness In. = 750 μ A Frequency0	Supply Voltage.,75VDD = 13.2VImage: Constraint of the second stress of the seco	Supply Voltage.,75 VDD = 13.2V 13.2 Supply Current VDD = 13.2V 7 Input Voltage Logical "0" Level \pm 10µA Input Bias - 0.3 0.08 Logical "1" Level $4.75 \le V_{DD} \le 5.25$ 2.2 VDD Brightness Input Current (note 2) 0 0.75 Brightness Input Voltage (pin 13) Input Current = 750µA, Tamb = 25°C 3 4.3 Off State Out. Voltage VO = 3V 13.2 18 Out. Sink Current (note 3) VO = 3V 10 10 Segment OFF VO = 1V (note 4) 10 10 Brightness In. = 0µA 0 10 10 Brightness In. = 750µA 12 15 25

Note: 1. Output matching is calculated as the percent variation from I $_{MAX}$ + I $_{MIN}$ /2.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40mA.

4. The VO voltage should be regulated by the user.

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FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate 31/ 2 digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing nonmultiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in Figure 3. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.

There is an internal limiting resistor of 400 Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.



There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5MHz is assumed.

Table 3 shows the Output Data Format for the M5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the cur-

rent per output, or operate the part at higher than 1V $V_{\mbox{OUT}}.$

The following equation can be used for calculations.

 $\label{eq:time_transform} \begin{array}{l} T_{j} = [\ (V_{OUT}) \ (I_{LED}) \ (No.of \ segments) + V_{DD} \ . \ 7 \ mA] \\ (132 \ ^{\circ}C/W) \ + \ T_{amb} \end{array}$

where:

 T_j = junction temperature (150 °C max)

 V_{OUT} = the voltage at the LED driver outputs $I_{I ED}$ = the LED current

132 °C/W = thermal coefficient of the package T_{amb} = ambient temperature

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Figure 5.



Table 3. Serial Data Bus / Outputs Correspondance

																			A. 1	
5451	35	34	33	32	31	30	29	28	3	27	26	25	24	23	3	22	21	20	19	START
5480	Х	23	22	21	20	19	Х	Х		18	Х	17	16	1:	5	14	13	12	х	START
5451	18	17	16	15	14	13	12	11	10	9	9	8	7	6	5	4	3	2	1	START
5480	Х	Х	Х	11	10	9	8	Х	Х)	κ .	7	6	5	4	3	2	1	Х	START
TYPICAL APPLICATION																				
i igule o	Figure 6. Basic 3 1/2 Digit Interface																			

TYPICAL APPLICATION

Figure 6. Basic 3 1/2 Digit Interface



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

Figure 7.



In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

$$R = \frac{V_{C} - V_{DMAX} - V_{OMIN}}{N_{MAX}L_{D}}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.

Figure 8.



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

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PART NUMBERING

Table 4. Order Codes

Part Number	Package	Temperature Range			
M5480	PDIP28	-25 to 85 °C			

obsolete Product(s). Obsolete Product(s)

PACKAGE MECHANICAL

Table 5. PDIP28 - Mechanical Data

Symbol		millimeters		inches					
	Тур	Min	Max	Тур	Min	Max			
a1		0.63			0.025				
b		0.45			0.018				
b1	0.23		0.31	0.009		0.012			
b2		1.27			0.050				
D			52.58			2.070			
E	15.2		16.68	0.598		0.657			
е		2.54			0.100				
e3		48.26			1.900				
F			14.1			0.555			
i		4.445			0.175				
L		3.3			0.130				

Figure 10. PDIP28 - Package Dimensions



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Note: Drawing is not to scale

REVISION HISTORY

Table 6. Revision History

Date	Revision	Description of Changes
May-1993	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

obsolete Product(s). Obsolete Product(s)

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