OptiMOS(TM)3 Power-Transistor

Features

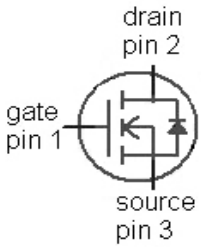
- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	3.4	mΩ
I_D	100	A

RoHS

Type	IPD034N06N3 G
	
Package	PG-TO252-3
Marking	034N06N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	100	A
		T_C=100 °C	100	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	400	
Avalanche energy, single pulse	E_{AS}	I_D=100 A, R_{GS}=25 Ω	149	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	167	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22
[2] Current is limited by bondwire; with an R_{thJC}=0.9 K/W the chip is able to carry 164 A.
[3] See figure 3 for more detailed information
[4] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.9	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[5)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=93 µA	2	3	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	2.8	3.4	mΩ
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A	75	149	-	S

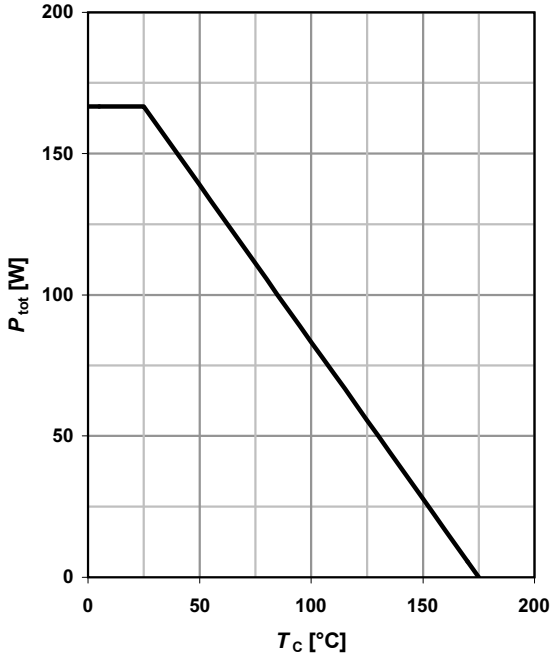
[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	8000	11000	pF
Output capacitance	C_{oss}		-	1700	2300	
Reverse transfer capacitance	C_{rss}		-	58	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=90 A, R_G=3.2 Ω	-	38	-	ns
Rise time	t_r		-	161	-	
Turn-off delay time	$t_{d(off)}$		-	63	-	
Fall time	t_f		-	16	-	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=100 A, V_{GS}=0 to 10 V	-	43	-	nC
Gate to drain charge	Q_{gd}		-	9	-	
Switching charge	Q_{sw}		-	28	-	
Gate charge total	Q_g		-	98	130	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	79	105	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	100	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=90A, di_F/dt=100 A/µs	-	48	-	ns
Reverse recovery charge	Q_{rr}		-	73	-	nC

[6)] See figure 16 for gate charge parameter definition

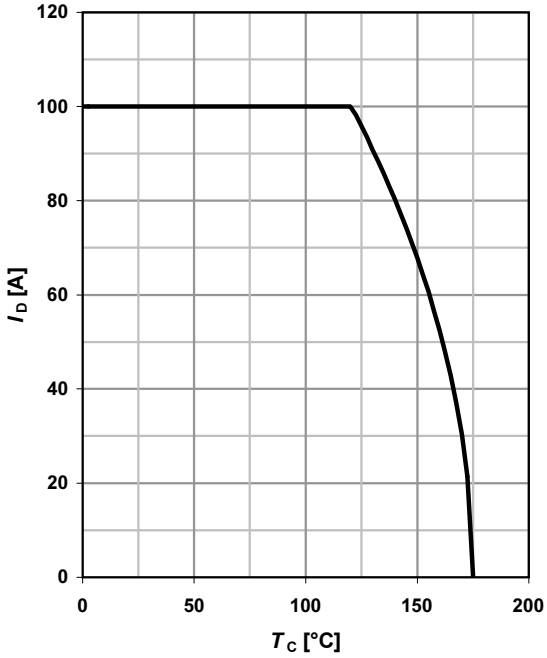
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

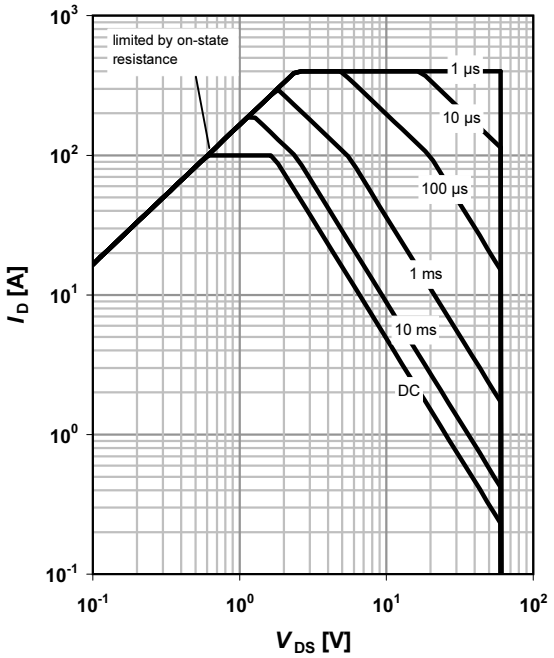
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

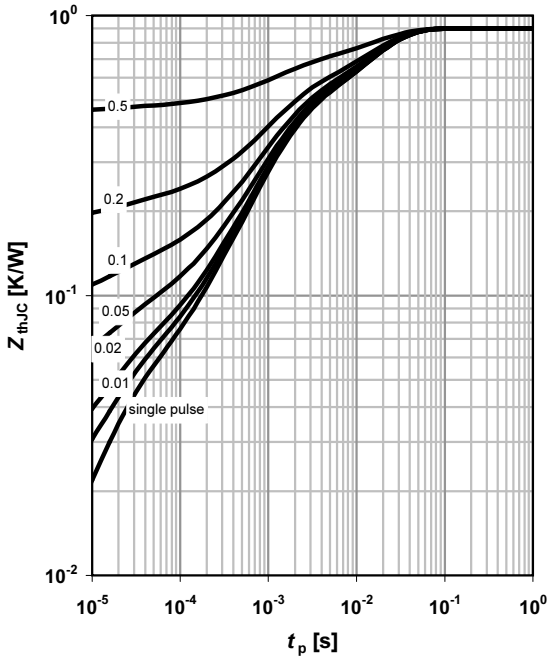
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

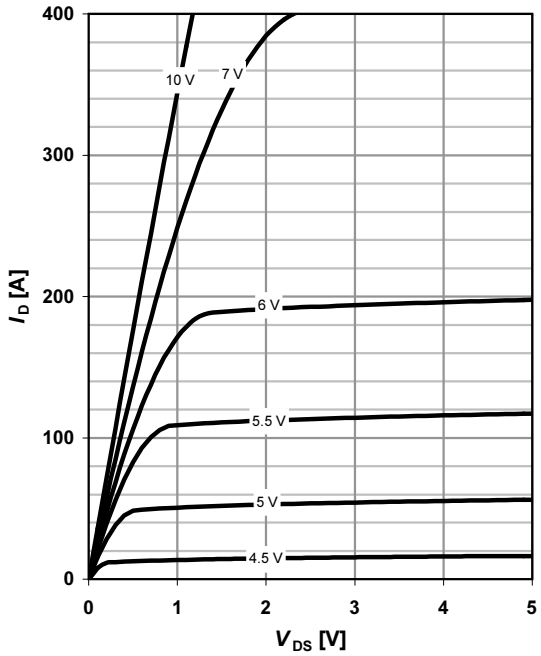
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

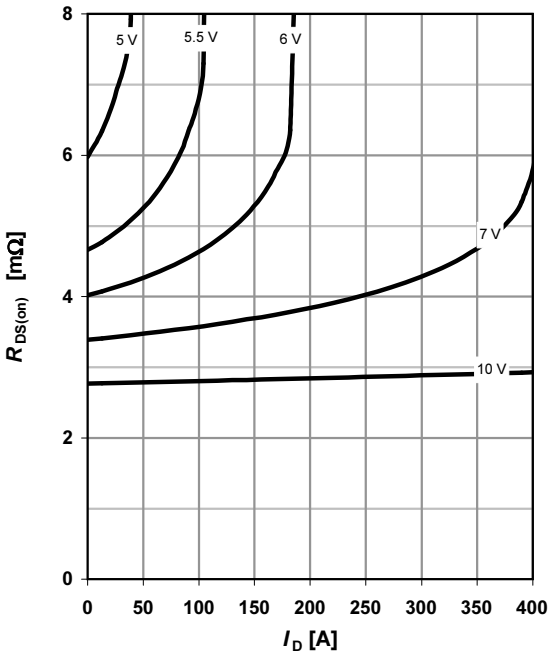
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

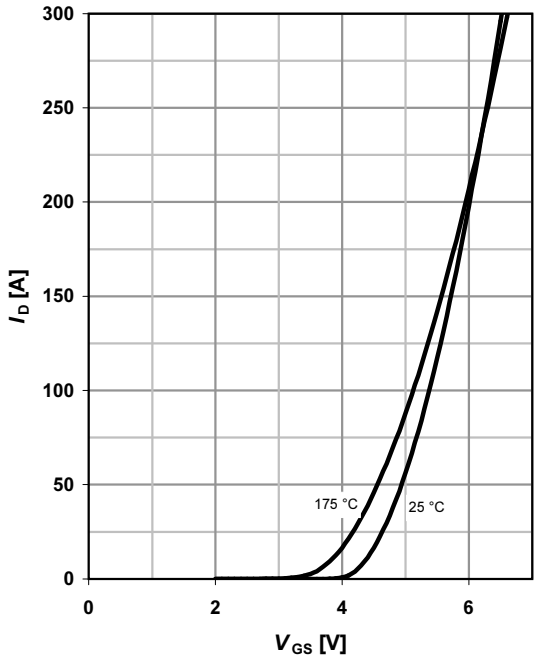
parameter: V_{GS}



7 Typ. transfer characteristics

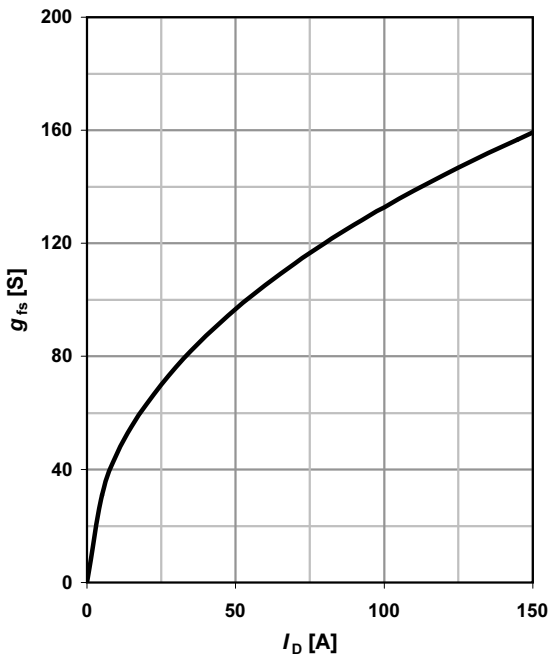
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



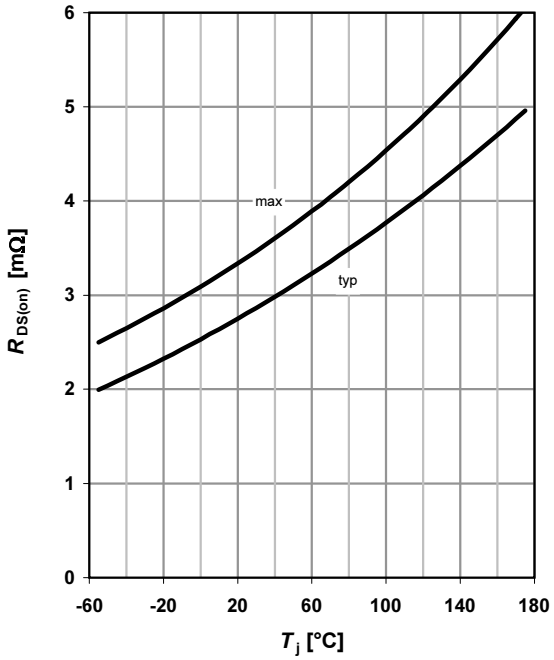
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

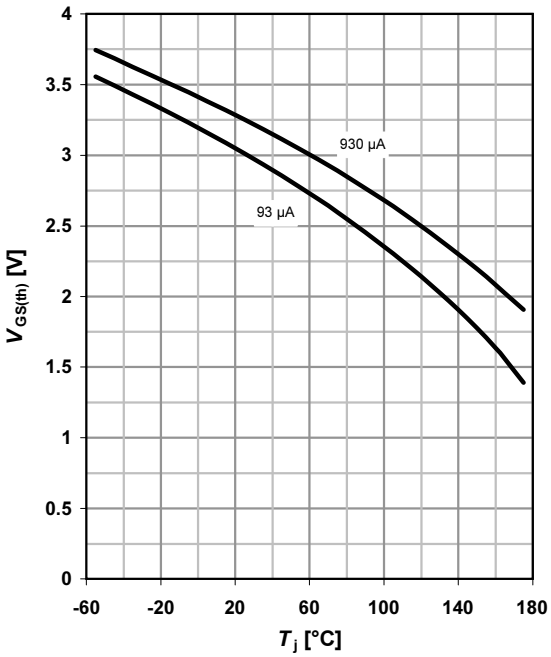
$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V



10 Typ. gate threshold voltage

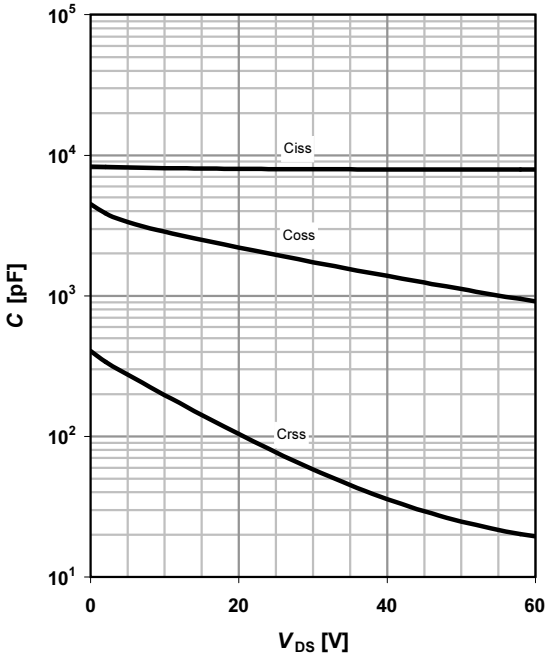
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

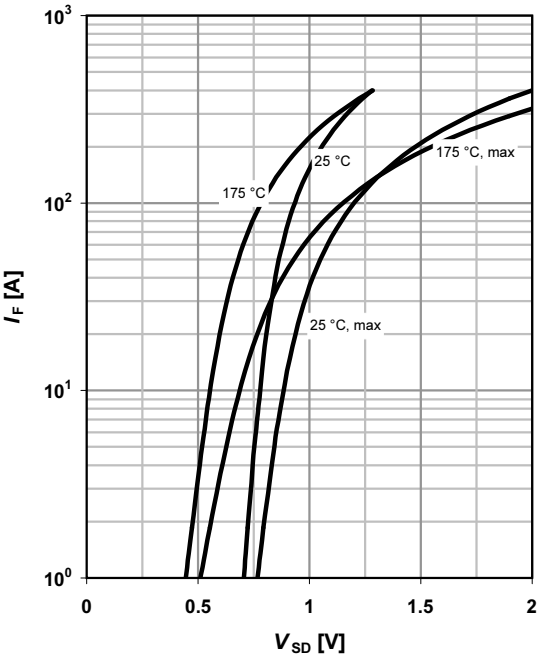
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

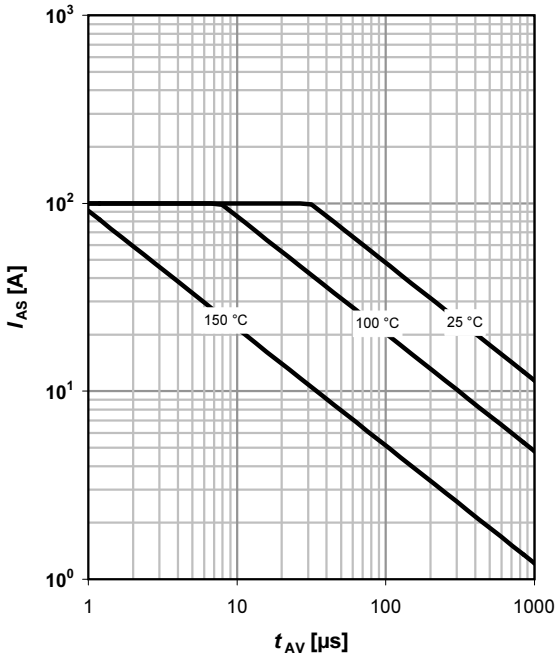
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

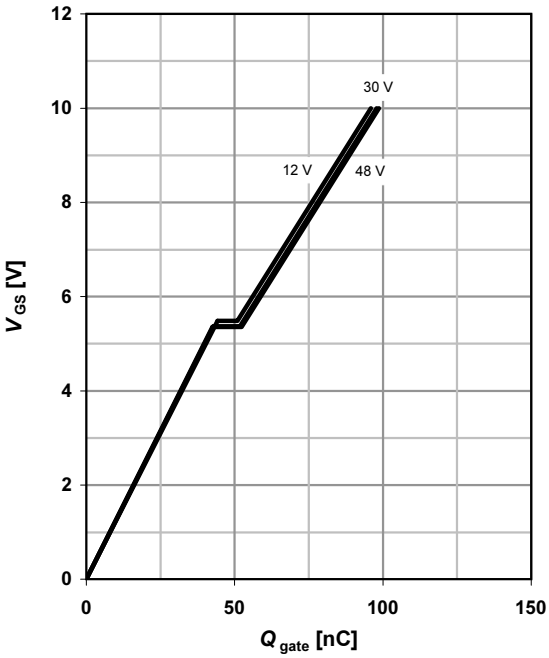
parameter: $T_{j(start)}$



14 Typ. gate charge

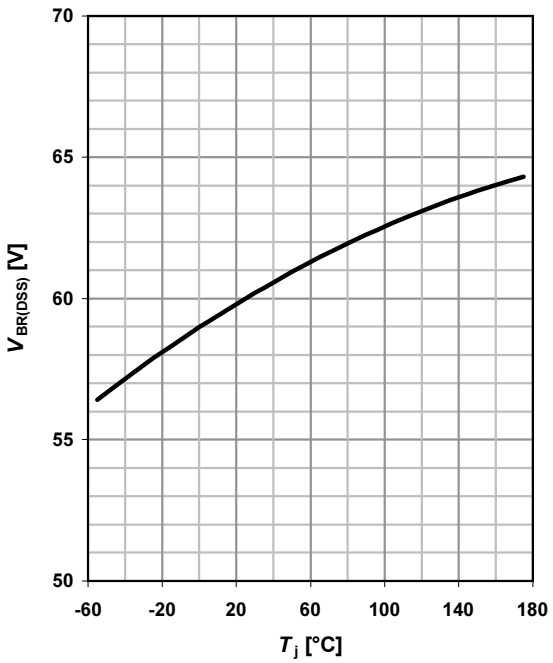
V_{GS}=f(Q_{gate}); I_D=100 A pulsed

parameter: V_{DD}

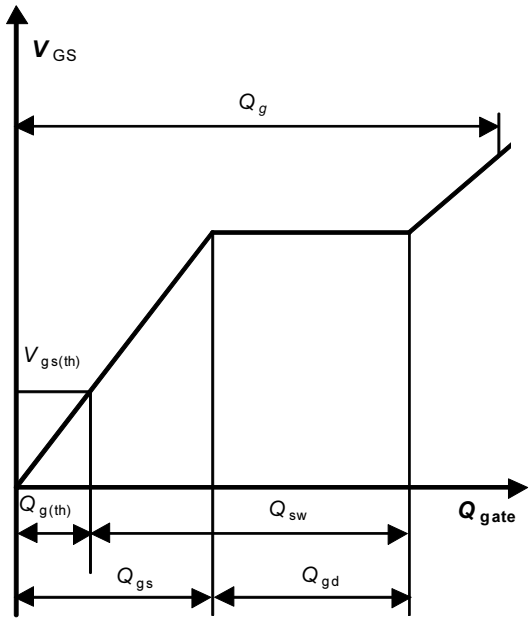


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



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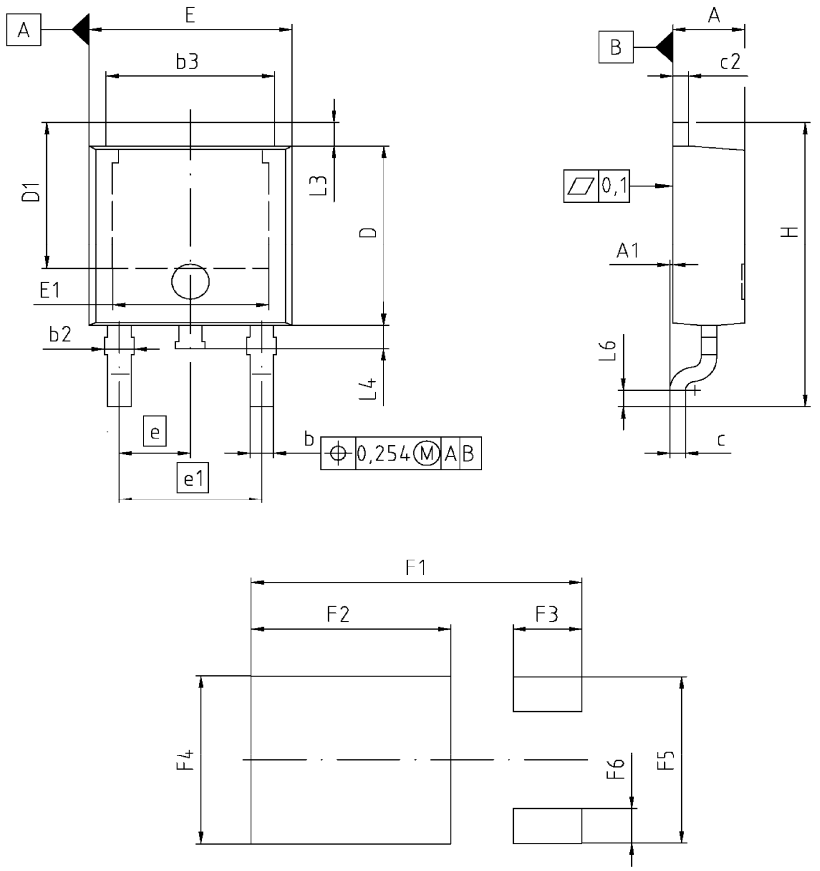
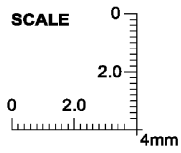


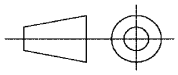
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.159	2.413	0.085	0.095
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.026	0.045
b3	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.842	0.198	0.230
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
H	9.400	10.480	0.370	0.413
L3	0.900	1.143	0.035	0.045
L4	0.584	0.950	0.023	0.037
L6	0.510	0.686	0.020	0.027
F1	10.500	10.700	0.413	0.421
F2	6.300	6.500	0.248	0.256
F3	2.100	2.300	0.083	0.091
F4	5.700	5.900	0.224	0.232
F5	5.660	5.860	0.222	0.231
F6	1.100	1.300	0.043	0.051

REFERENCE
JEDEC TO252

SCALE



EUROPEAN PROJECTION



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